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Editorial

Selected Papers from the Southern Programmable Logic Conference (SPL2010)

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This is the third special issue published in this journal with selected contributions from the VI Southern Conference on Programmable Logic (SPL, www.splconf.org). SPL is one of the first-class conferences on programmable logic around the world. Started in 2005, SPL has since 2007 the technical cosponsorship of the IEEE Circuits and Systems Society (CAS). The conference has been always organized in the south hemisphere. The selection of papers presented in this special issue is coming from the last 6th edition, held in Ipojuca, Brazil, from March 24 to 26, 2010.

This issue is focused on speech and video acceleration applications. The first paper by P. Eh Kan et al., "*FPGA implementation for GMM-based speaker identification*" in the area of biometric-based speaker identification, describes the hardware implementation for classification of a text-independent (Gaussian mixture model) GMM-based speaker identification system. Authors show that the proposed hardware implementation allows simultaneous identification processing for a large number of voice streams in real time.

In "*FPGA implementation of a pipelined Gaussian calculation for HMM-based large-vocabulary speech recognition*," R. Veitch et al. present several alternatives for a Gaussian core as part of a larger speech recognition system. These cores are developed as an embedded peripheral and as a scalable, parallel hardware accelerator.

Next, in "A *high throughput hardware architecture for the H.264/AVC half-pixel motion estimation targeting high definition videos*," M. M. Corrêa et al. present a high-performance hardware implementation for the H.264/AVC half-pixel motion estimation that targets high-definition videos. This design can process very high-definition videos like QHDTV (3840×2048) in real time (30 frames per second).

E. C. Pedrino et al. in the area of computer vision presented "*A genetic programming approach to reconfigure a morphological image processing architecture*." They report the development of a reconfigurable architecture using logical, arithmetic, and morphological instructions generated automatically by a genetic programming approach.

Related to cryptographic algorithms, G. Perin et al., in "*Montgomery modular multiplication on reconfigurable hardware: systolic versus multiplexed implementation*," develop two Montgomery modular multiplication architectures: a systolic and a multiplexed circuit with competitive results.

Finally, A. G. Silva-Filho et al. presented an advanced EDA tool in the paper "*An ESL approach for energy consumption analysis of cache memories in SoC platforms*" in the area of design space exploration. They propose an electronic-system-level (ESL) approach for system modeling and cache energy consumption analysis of SoCs.

Acknowledgments

The authors would like to express their sincere thanks to the reviewers for their hard work, to Dr. René Cumplido, the Editor-in-Chief, and to the editorial staff at Hindawi. They hope that you enjoy this special issue and that it inspires more research to overcome future challenges in the areas related to programmable logic and its applications.

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