Digital Control Implementation to Reduce the Cost and Improve the Performance of the Control Stage of an Industrial Switch-Mode Power Supply

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Abstract **The main objective of this work is the design and implementation of the digital control stage of a 280W AC/DC industrial power supply in a single low-cost microcontroller to replace the analog control stage. The switch-mode power supply (SMPS) consists of a PFC boost converter with fixed frequency operation and a variable frequency LLC series resonant DC/DC converter. Input voltage range is $85V_{RMS}$-$550V_{RMS}$ and the output voltage range is 24V-28V. A digital controller is especially suitable for this kind of SMPS to implement its multiple functionalities and to keep the efficiency and the performance high over the wide range of input voltages. Additional advantages of the digital control are reliability and size. The optimized design and implementation of the digital control stage it is presented. Experimental results show the stable operation of the controlled system and an estimation of the cost reduction achieved with the digital control stage.**

I. INTRODUCTION

Nowadays, around 90% of the commercial SMPSs in the low and medium power range have an analog control stage. Main factors that have limited a wider use of digital control are the cost, the power consumption of the digital devices, especially for low power SMPS, and the little experience of the designers. However, this trend has changed during recent years and nowadays digital control is becoming more competitive compared to the classical analog control ([1], [2]).

In the state of art several solutions can be found in recent years that propose a digital implementation of the control stage of a SMPS. In [3], [4], new techniques are proposed and implemented in a simple topology using an FPGA, a high cost solution because of the chip and the peripherals needed (ADC, oscillator…). In [5], [6] a high performance DSP (TMS320F2808) is used for switching frequencies of 12kHz and 200kHz to control a three phase boost rectifier and a buck converter respectively. In [7], two low-cost low-precision PIC16F876 are used to control an UPS with PFC.

In this paper it is proposed to use a lower-cost (compared to the previous solutions) single DSC (Digital Signal Controller) to control a more complex SMPS. The main challenge of this work is to achieve the synchronization of the measurements and calculations of the two-stages of the SMPS, a three-level PFC boost with a fixed switching frequency of 75kHz [8] and resonant DC/DC converter [9] with a variable switching frequency up to 190kHz, in a single low-cost MCU. The selected digital signal controller (DSC), in the market since the end of 2008, has the advantages of a low price and highly optimized characteristics to control a SMPS. Using this DSC and the optimized digital control design, explained later, it has been demonstrated to be feasible the reduction of the cost and the improvement of the performance of the control stage of the two-stage commercial AC/DC SMPS.

II. SYSTEM DESCRIPTION

The main characteristics of the SMPS are a high power density, a high efficiency and a very wide input voltage range, $85V_{RMS}$ -$550V_{RMS}$, due to the market demand of this kind of AC/DC SMPS. It consists of two stages: A PFC three-level boost converter and a resonant LLC series DC/DC converter as it can be seen in Figure 1. The PFC stage operates at a fixed frequency of 75kHz. The second stage works at a variable frequency from 140kHz (28V) to 190kHz (24V) and the control stage is independent of the first stage control. The maximum nominal output power is 280W. In order to comply with these specifications, the SMPS has several operating modes and multiple functionalities to keep the performance and the efficiency high over the whole input voltage range. As a consequence, the analog control stage requires additional components that increase the size, the cost and the power consumption and decrease the reliability. Due to the necessity of a cheaper,

simpler and smaller control stage, a digital control implementation has been considered. Additionally, a digital control stage allows an improved performance: jittering (first stage) to reduce the EMC levels, higher reliability and better temperature and failure testing.

The objective of this work is the digital control implementation to replace the analog control stage including all its functionalities at a lower cost. It is also implemented the jittering functionality that improves the performance of the analog control stage.

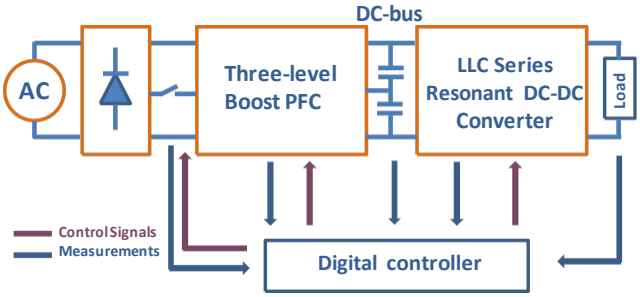

Figure 1. Block diagram of the system

III. CONTROL STAGE DESIGN

The control stage of this power supply consists of three main control loops:

- A fast current loop in the first stage to achieve a high power factor
- A slow voltage loop in the first stage to balance the energy taken from the AC mains (like in any PFC)
- A very fast voltage loop of the output voltage of the converter to feed the load with fast dynamics

To comply with all the functionalities of the SMPS, the following measurements have to be done:

- First stage: Input voltage (full rectified and positive), feedforward input voltage (V_{ff}), voltage of the two dc-bus capacitors and input current.
- Second stage: Resonant tank current and a control signal for the voltage loop.

As a conclusion, seven ADC inputs and a comparator (as the resonant tank current does not need such a high precision to implement the overload protection) and seven control signals (six DPWM, two for the first stage, four for the second stage and a control signal for the input switch) are needed.

The PFC stage regulators have been designed in Matlab-Simulink and the validation of the averaged model has been done using Pspice. The discretization of the regulators (both PID) has been done with zero order hold. This method is less time consuming than other alternatives but adds phase to the bode plot response in frequencies close to the sampling frequency, which has to be considered in the design of the control loops to avoid instability. The bandwidths of the voltage and current loop are 6Hz and 10kHz respectively.

Due to the high input voltage range $85V_{RMS}$-$550V_{RMS}$ and to keep the efficiency high, the SMPS has several operation modes. In the different operation modes the topology and/or the operating conditions are modified. To obtain both stability and high power factor, the current regulator has been optimized for the input voltage range that corresponds to each operation mode. Moreover, for the operation modes with higher input voltage range, more than one current regulator has been designed. The control signal which is used in the implementation of this algorithm is the feedforward (V_{ff}) voltage, already measured for the input V_{ff} compensation of the current loop. An hysteresis band has been included to avoid switching between different operational modes due to a unexpected noise in V_{ff}.

The resonant DC/DC stage is controlled by a voltage loop with frequency regulation. A voltage to frequency converter has been designed and implemented for the design of this stage control as the analog implementation of the first stage of the controller can be done with simple and cheap components. The digital implementation can be done with a function or a look-up table. The first option has been chosen (first order function) as it needs less memory size and it is also less time consuming (225ns vs 420ns obtained experimentally). A dead band time for the control signals of this stage is also implemented. Despite this control stage is not fully replaced, several operational amplifiers, logic components and signal diodes, resistors and capacitors used to generate the control signals for the different operation modes can be suppressed in the digital implementation.

Overvoltage and short-circuit protections and a soft-start transient have been implemented.

The state of the input switch and the DC-bus capacitors voltage (380V-780V) (Figure 1) is set depending on the feedforward input voltage value, configuring the mode of operation in an initialization task that lasts several line periods. A synchronization algorithm of the control signals with the input voltage for the mode of operation that requires it has also been included. The compensation of the DC-bus capacitors voltage, of low dynamic behavior, avoids the damage of one of the capacitors due to a voltage unbalance.

In order to reduce the EMI levels and therefore to reduce the EMI filter a jittering algorithm, not implemented in the analog control stage, has been included in the digital controller of the first stage. Instead of controlling the PFC stage with a fixed period of 75kHz, several frequencies slightly under 75kHz are used. It has been considered a pseudo-random function to generate the operating frequencies for the PFC stage.

An additional issue of the discrete design domain, the conditions to avoid limit cycles, has been considered in the design process to avoid instability [10]. It has also been considered the effect of the delay between an ADC measurement and the application of the next duty cycle,

which can produce an unexpected phase decrease at high frequencies.

IV. Digital Control Implementation

The digital controller has been selected according to the main criteria of cost. Other parameters such as resolution and precision have also been analyzed. The best candidates from all the analyzed devices have been found among the DSC (hybrid device between a Digital Signal Processor, DSP, and a Microcontroller Unit, MCU) and finally TMS320F28027 TI 32-bits fixed point DSC [11] has been selected as the best candidate for this application.

Main characteristics of the selected DSC are:

- 60MHz CPU speed
- 32-bit fixed point precision
- 12-bit precision ADC
- Four ePWM modules (with two channels each)
- Two analog comparators
- Three timers

One of the main limitations of this controller, compared to the analog control alternative, is the small measurement range (0V-3.3V), as the analog control stage handles in this SMPS voltages up to four times higher. To compensate this drawback, and taking into account that the converter has different operation modes, it has been designed a variable gain for the input voltage measurement. It has been done with a simple low cost-low consumption circuit. To the input resistive divider it has been added a two parallel branches that consist of a resistor and a grounded bipolar transistor. When needed, a parallel branch can be added by closing the transistor, adding a resistor in parallel and modifying the gain to comply with the measurement range. The signal to drive the transistor can be generated from the digital controller due to the low gate current consumption.

The PFC stage is controlled by two loops with different dynamic behavior. As the voltage loop has a slower dynamic behavior than the current loop, it does not need to be updated each switching cycle, and the calculations can be divided in several periods, achieving a reduction in the mean computation time of each switching period. This algorithm has been tested for ten switching periods and satisfactory results have been obtained.

To reduce the measurement time, the input signals have been divided in several groups depending on the rate of measurement (output voltage control signal: very fast, at the rate of the second stage switching frequency; input current and input voltages: fast, at the rate of the first stage; feedforward voltage and DC-bus capacitors voltages: slow and finally the mean value of the resonant current, which is connected to an analog comparator included in the DSC).

To decrease the computation time of the DSC tasks it has been used the IQMath library [12], which optimizes the calculations implemented with floating data (regulators final consumption time is 1µs approximately, obtained experimentally).

The design of the digital control stage could be done for each stage independently, with a specifically selected DSC for each stage. Even though, from the cost point of view, it would be a better option to include both control loops in a single digital controller. This is not simple due to the different dynamic behavior of each stage of the SMPS, fixed 13.3µs switching period for the first stage and variable period from 5µs to 8µs for the second stage. To synchronize the tasks of both stages, it has been considered the first stage measurements as the highest priority task (associated to timer 0, linked to ADC_ISR1 interruption). Taking this into account, the second stage measurement and calculations (waveform C in Figure 2) can interrupt the first stage calculations (timer 1, linked to ADC_ISR2) to achieve the measurements at the necessary rate (5µs-8µs), but always with less priority than timer 0 to avoid interference with the first stage measurements. With this strategy it is avoided oversampling, overlapping tasks and it is managed to get a new control signal each period of both stages.

The main disadvantage of this implementation could be that the measurement point of the second stage changes, as it can be seen in Figure 4 . However, as the measured signal in the second stage is a DC voltage, it does not affect the stability of the loop.

Other alternatives have been taken into account to synchronize both stages, as linking timer 1 interruption (ISR2) to the second stage control signal instead of using the first stage main ePWM signal. The main disadvantage of this strategy is that in some cases, three measurements of the second stage and one of the first stage would take place, with a high consumption of time. With the proposed strategy, the same functionality is done with only three measurement events.

Analyzing the waveforms of Figure 2, it can be seen the operation of the DSC as explained before.

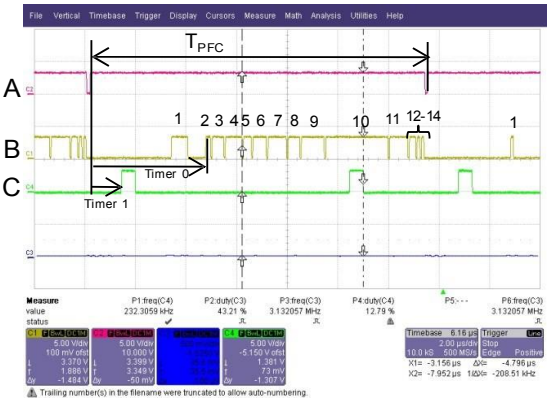

Figure 2. Experimental waveforms of the microcontroller tasks for the PFC loop and for the resonant DC/DC stage; (Time scale: 2µs/div; Voltage scale: 2V/div)

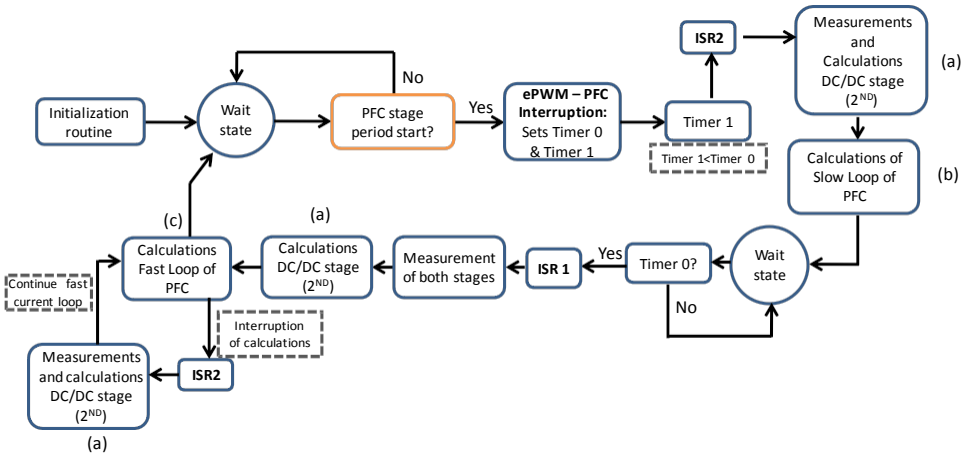

Figure 3. Flow diagram of the control algorithm

Two internal auxiliary signals (waveforms B and C in Figure 2) have been generated to control the length and position of each task of the microcontroller and it is set to high level (3.3V) when any computation of the DSC is being processed.

Waveform A of Figure 2 shows one of the two duty cycle signals of the PFC boost converter. Waveform C indicates calculations of the second stage and waveform B of the first stage except the task number four where the second stage calculation is placed (closer than 5µs to the previous and next second stage calculations)

The steps of the control stage algorithm (Figure 2) are: 1.-Partial calculation of the slow PFC loop; 2.-Partial calculation of the Jittering; 3.-ADC data acquisition (first and second stage measurements); 4.- Second stage calculations; 5-6.- Calculations of the current loop of the PFC stage; 7.- Digital filter for the input current; 8-9.- Current regulator; 10-11.- Jittering main calculations; 12.- DPWM conversion; 13-14: Synchronization algorithm of the control signals with the input voltage.

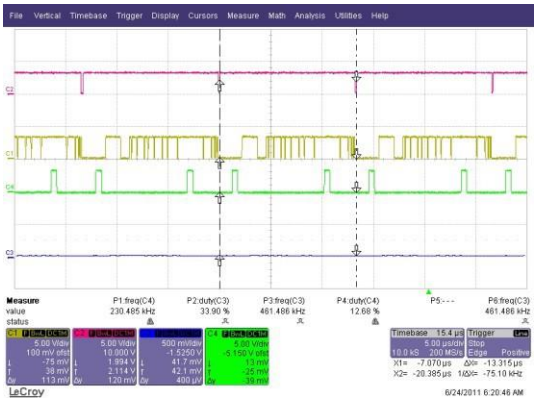

Figure 4. Experimental waveforms of the microcontroller tasks for the PFC loop and for the resonant DC/DC stage (several periods); (Time scale: 5µs/div)

For a better understanding of the control strategy it can be seen in Figure 3 the flow diagram of the control algorithm. Some restrictions have been taken into account in the implementation of the synchronization algorithm:

- Second stage duty cycle has to be updated three times per period (13.3µs) so each 2^{ND} stage period (5.26µs minimum) there is a new calculation of duty cycle and frequency.
- Priority of ISR1 > ISR2 > control calculations
- The PFC input current measurement is the highest priority task to avoid interference of the measurement point with the loop stability
- The measurement of the PFC stage control signals is done as close as possible to the end of the period to reduce delays between the measurement and the application of the new duty cycle

The DSC operation, shown in Figure 3, is the following: The rising slope of the ePWM module of the PFC stage calls the interruption ePWM1_ISR. This interruption sets the timers 0 and 1. Timer one begins first and call ISR2 that measures the second stage control signals. After the last measurement is done, ADC_ISR2 is called and the operations of the second stage are done.

After the first calculation of the second stage, some calculations (they are divided into ten periods) of the "slow loop" of the PFC stage are done. Then the DSC waits for timer cero. This timer calls ISR1 that measures both the first and the second stage control signals and calculate both stages control parameters.

During the calculations of the first stage, (task number ten in Figure 2), the measurement and calculations of the second stage are done again interrupting the first stage calculations to manage a measuring rate faster than 5.26µs.

In Figure 3 there are several blocks that consist of several tasks that have not been detailed in the flow diagram for a

better understanding. The tasks that are carried out in each one are:

a) Resonant DC/DC stage calculations:

- Digital filter of the control signal
- Calculations and assignations of the duty cycle and the operating frequency of the second stage
- Limitations/Protections

b) Slow PFC loop calculations:

- DC-bus capacitors compensation
- Voltage regulator
- Limitations/Protections
- Filter of feedforward voltage (V_{ff})

c) Fast loop calculations

- Tasks from two to fourteen of Figure 2, detailed before in this section

With the proposed control strategy it has been implemented successfully the control of the SMPS in one low-cost digital controller.

V. Experimental Results

Experimental results have shown the robust operation of the converter with the three loops. A digital control PCB has been implemented to replace the analog control stage in the commercial AC/DC SMPS. It includes a JTAG port to allow easy programming and debugging. In Figure 5 it can be seen the input current, where a power factor higher than 99% and a THD of 10% approximately has been achieved. In Figure 6 the output voltage and the capacitors voltages (with the voltage balancing algorithm) are shown. The balanced voltages of the DC-bus (with 1% of precision of the balancing algorithm) can be seen also in Figure 7, where it is shown also the DC-bus voltage.

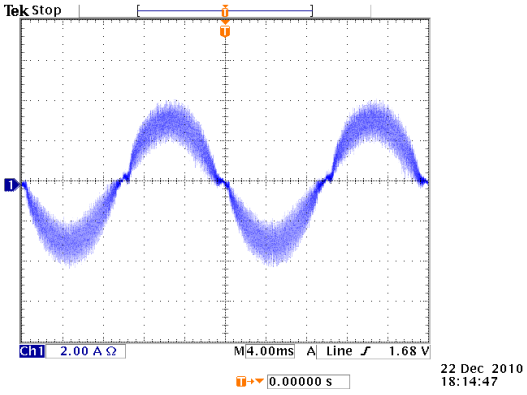

Figure 5. Measured input current of the SMPS (2A/div and 4ms/div)

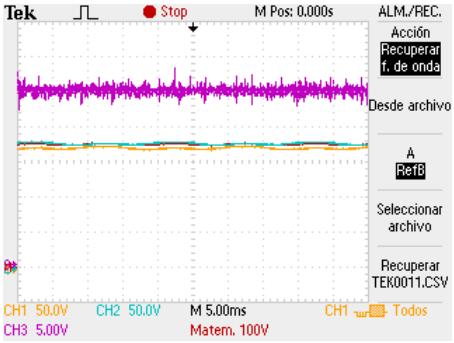

Figure 6. Measured output voltage (5V/div) and DC-bus capacitors voltage (50V/div and 5ms/div)

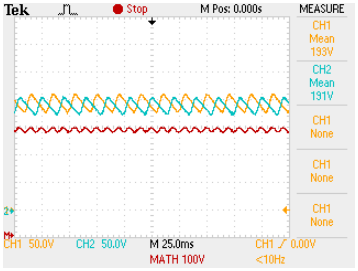

Figure 7. Output voltage (100V/div) and DC-bus capacitors voltage (50V/div and 25ms/div) at 280W of output power and 85V_{RMS} input voltage

Tests on the second stage show good regulation in all the operating range. In Figure 8 the resonant current for an output voltage of 24.8V is shown.

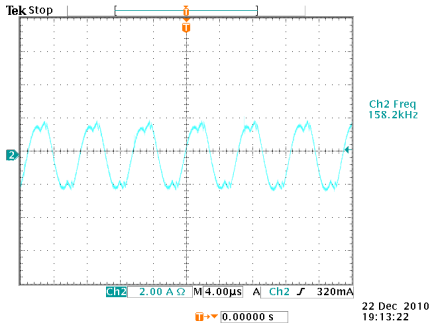

Figure 8. Measured resonant current of the DC/DC stage (2A/div and 4µs/div)

Figure 9 shows the photograph of the SMPS and Figure 10 (from top to bottom) shows control signals for both stages: the duty cycles of the first stage in one of the operating modes and the control signal of the second stage loop (5ms/div). In this figure the correct synchronization of the duty cycle signals with the half-line period can be appreciated. Figure 11 shows a photograph of the digital control PCB that has been designed, implemented and tested.

It has been estimated, for big quantities (>kU), that the cost of the digital control stage is 35% of the cost of the analog control suppressed components: three IC controllers (most expensive components) and several operational amplifiers, logic components, capacitors and resistors.

Figure 9. Photograph of the SMPS

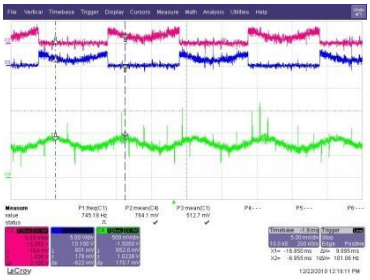

Figure 10. Experimental control signals of three level boost control signals (5V/div) and output voltage loop control signal (500mV/div); Time scale 5ms/div

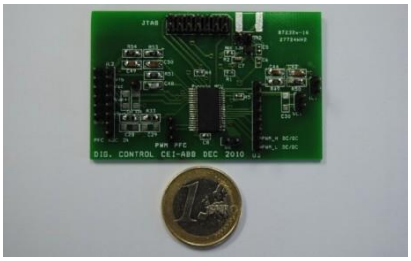

Figure 11. Photograph of the digital control PCB

Additionally, the consumption of the digital controller (only the chip and the voltage regulator (5V to 3.3V)) is 1W, 0.36% of the total output power, which does not contribute significantly to the consumption of the SMPS.

VI. CONCLUSIONS

In this paper the digital control stage to replace the analog control stage of an industrial AC/DC power supply is presented. The power supply consists of two stages, a fixed frequency PFC boost converter and a variable frequency DC/DC resonant converter. The main challenge of the project has been to develop a digital control stage with multiple functionalities (including the design of three loops, multiple functionalities and the protections) in a single low-cost microcontroller. The digital control design and the optimized implementation in the microcontroller are described. All the functionalities of the analog control stage are included in the digital control stage and also a new functionality is added: the jittering capability, which decreases the EMI levels. An estimation of the cost reduction is presented, achieving a 65% reduction compared to the cost of the suppressed components of the previous analog solution. The consumption of the DSC and of the additional components needed is only 0.36% of the total consumption of the SMPS. Experimental results show successful results in the tests of the commercial SMPS using a single low-cost DSC and a few additional low-cost components.

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