Autotuning digital controller for current sensorless power factor corrector stage in continuous conduction mode

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Abstract— **A circuit that compensates the volt-seconds error across the inductor in current sensorless digital control for continuous conduction mode power factor correction (PFC) stage is presented. Low cost ad-hoc sigma-delta analog to digital converters (ΣΔ ADCs) are used to sample the PFC input and output voltage. Instead of being measured, the input current is estimated in a digital circuit to be used in the current loop. A nonlinear carrier control is implemented in the digital controller in order to obtain the power factor correction. Drive signal's delays causes differences between the digital current and the real current, producing that volt-seconds error. The control algorithm is compensated taking into account the delays. The influence of a wrong compensation is presented. Experimental results show power factor values and harmonic content within the IEC 61000-3-2 Class C standard in different operation conditions. Furthermore, the use of this PFC stage for electronics ballast to compensate the effect of the utility voltage fluctuation in HID lamps is also verified taking advantage of the digital device capabilities.**

Keywords-power factor correction; Nonlinear-carrier control; rebuilt current, autotuning digital controller, light flickering

I. INTRODUCTION

In some previous work [1], a current estimation technique, so called current rebuilding technique, was used to avoid the current sensor in PFC circuits, resulting in the proposal whose block diagram is shown in Fig. 1. Both, current and output loops are employed, substituting the current measurement by the digitally rebuilt current. Precedents of variable estimation or sensorless control are found in [2-3] where the input voltage is not measured, while in [4-6] the current is not measured and no current loop is used. In [7], a digitally emulated current mode control for DC-DC boost converter using an FPGA is proposed without a high cost A/D converter for the input current. A derivation of the input current with a Kalman filter is presented in [8] for a DC-DC boost converter too. The current rebuilding technique uses ADCs that are *ad-hoc* designed to be highly integrated in the digital circuit. They measure the input and output voltages (v_{in} and v_o). This is possible since the measured voltages have slow dynamics (50-60 Hz).

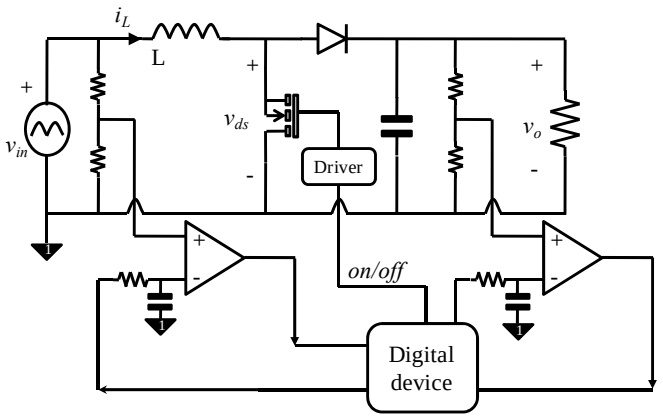

Figure 1. Experimental PFC circuit and control schematic.

A peak-current non-linear carrier control [9-10] is implemented in a digital device in order to achieve the power factor correction. Because of the delay between the transient of the drive signal and the effective change of the voltage across the inductor, the control algorithm must be compensated in order to apply the volt-seconds in the on and off times of each switching period that result in the desired current shape.

An auxiliary circuit detects the voltage transitions when the on/off and the off/on switch occurs. This circuit adapts the MOSFET drain-to-source voltage to a digital input. Then, the delay with respect the drive signal generated by the digital control algorithm is computed. The measurement of these delays is used to select the compensation value for the control algorithm. A comparison between the case of using automatic compensation (autotuning) and manually preset compensation values is presented.

Finally, the autotuning PFC circuit with the described digital controller is used as a front-end stage for a HID lamps electronic ballast. Making the most of the digital device

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capabilities, a voltage controller that selects one out of two possible gains has been implemented to eliminate the lamp light flickering during utility voltage fluctuations with a small PFC stage output capacitor.

II. CONTROL ALGORITHM

Nonlinear-carrier (NLC) control [10] is used to shape the input current. This controller compares a carrier signal with the variable under control (rebuilt input current) in the boost PFC. Finite-difference equations to calculate the input (inductor) current (1) and (2) are implemented in the digital circuit.

- *On-time:*

$$i_L(k+1) = i_L(k) + \frac{v_{in}}{L}\Delta t \tag{1}$$

- *Off-time:*

$$i_L(k+1) = i_L(k) + \frac{v_{in} - v_o}{L}\Delta t \tag{2}$$

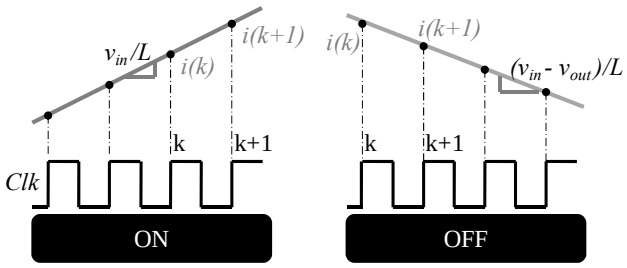


Figure 2. Rebuilding current concept

Fig. 2 shows the current rebuilding concept according to (1) y (2). Since current calculation frequency is the frequency of the digital device clock signal, it determines the current resolution for a given voltage operation conditions.

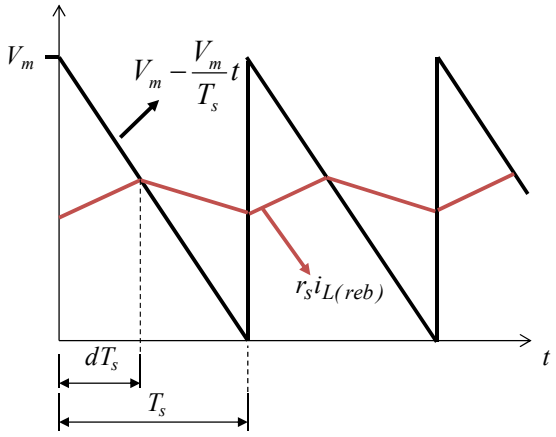


Figure 3. NLC control algorithm

The rebuilt peak current follows the input voltage in each switching period as is described in [9-10]. The comparison between a sawtooth function and the rebuilt input current ($i_{L(reb)}$) determines the duty cycle (d) in each switching period. Fig. 3 shows the triangular carrier function, which has a peak value of V_m. This value is controlled by the outer voltage loop.

The turn-off instant corresponds to (3), and in a boost converter can be rewritten as (4), and, therefore, the peak current follows the input voltage in each switching period.

$$V_m - V_m \frac{t_{on}}{T_s} = r_s \hat{i}_{L(reb)} \tag{3}$$

$$V_m \frac{v_{in}}{V_o} = r_s \hat{i}_{L(reb)} \tag{4}$$

being T_s the switching period and r_s the virtual current sensor resistor.

In the algorithm, negative values of the digitally rebuilt current are not allowed. During the off-time, if equation (2) gives a negative value, it is forced to zero leading to discontinuous conduction mode (DCM) in the digitally rebuilt current. A signal denominated $Mode_{Dig}$ shows this DCM condition in the algorithm, being "1" when a DCM switching period is detected (Fig. 4).

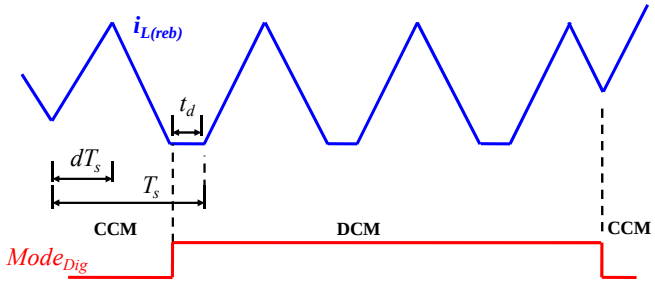


Figure 4. DCM detection signal in the digitally rebuilt current

Using the original NLC, the average rebuilt current in the switching period, T_s, $\langle i_{Lreb} \rangle_{Ts}$, takes the shape of the input voltage in CCM [10]. For the general case

$$\left\langle i_{L(reb)} \right\rangle_{T_s} = \left\langle i_{L(reb)CCM} \right\rangle_{T_s} \left(1 - \frac{t_d}{T_s}\right), \tag{5}$$

t_d being the time when $i_{L(reb)} = 0$ within the switching period, so when the DCM condition occurs ($Mode_{Dig}$ = "1"), even in the case of perfect matching between the actual an the rebuilt currents, the average input current does not exactly follow the input voltage.

If DCM detection based on the rebuilt signal matches in a high degree the actual DCM case then the rebuilding algorithm finds a true or almost true value $i_L = i_{L(reb)} = 0$ at the beginning of the switching period, reducing the volt-second error accumulation in the utility semi period.

III. DRIVE SIGNAL'S DELAYS

Drive signal's delays are the main cause of the accumulative inductance volt-seconds error. With this, the volt-seconds across the inductor in each switching period are different to the calculated theoretical values. Therefore, the real input current does not grow as the digitally calculated input current.

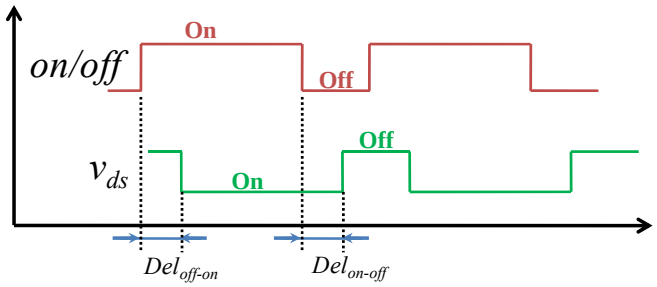


Figure 5. Drive signal's delays diagram ($Del_{on\text{-}off}$ y $Del_{off\text{-}on}$).

Fig. 5 depicts these drive signal's delays causing the volt-seconds across the inductance to be different from the digitally calculated (theoretical) value. The original control algorithm is modified to use the measured time difference and self-compensates the duty cycle in each switching period (73.2 kHz in this case). The compensation technique can be complemented introducing an offset in the compensation time, to take into account the input and output voltage acquisition errors that make a difference between the calculated voltage across the inductor and the real one.

The NLC control algorithm compensation is achieved advancing the *on/off* signal with respect the theoretical one. Fig. 6 shows this compensation with $C_{on\text{-}off}$ and $C_{off\text{-}on}$ times. Taking into account the delays shown in Fig. 5, an ideal compensation would be achieved when $C_{on\text{-}off} = Del_{on\text{-}off}$ and $C_{off\text{-}on} = Del_{off\text{-}on}$. Then, the FPGA generates the "compensated" signal instead. Once the *on/off* signal travels through the driver and switch, the real pulses will be almost identical to the "non-compensated" signal, which is the desired behavior.

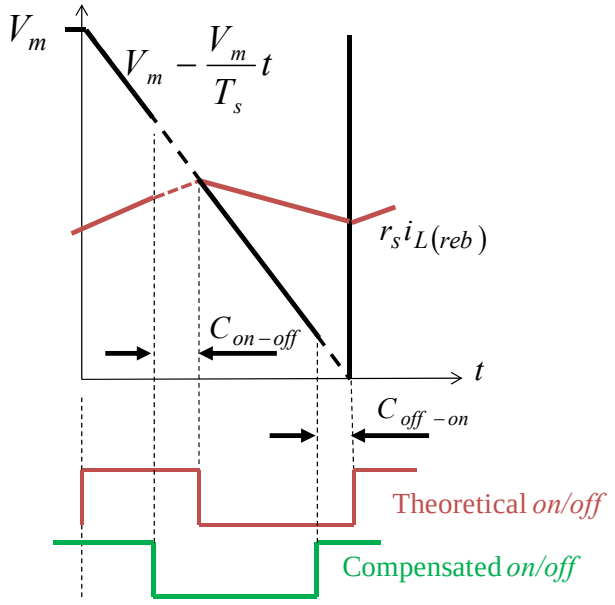


Figure 6. Compensated NLC control algorithm

The difference between the measured delays (Del_x) and the implemented into the compensation delays (C_x) would cause errors in the input current. It is defined the time compensation error, Δt_{onoff} and Δt_{offon}, where:

$$\Delta t_{on-off} = Del_{on-off} - C_{on-off} \tag{6}$$

$$\Delta t_{off-on} = Del_{off-on} - C_{off-on} \tag{7}$$

In [1] the expression that defines the current distortion created by these compensation errors (i_{ind}) is determined.

$$i_{ind} = \frac{1}{\omega L}\left\{\hat{V}_{in}\cos(\omega t) - \hat{V}_{in}\cos\left[\omega\left(t+\Delta T_s\right)\right] + V_o\omega t(\Delta d)\right\} \tag{8}$$

where $\Delta d = \left(\Delta t_{on-off} - \Delta t_{off-on}\right)/T_s$ accounts the duty cycle modification, and $\Delta T_s = \left(\Delta t_{on-off} + \Delta t_{off-on}\right)/2$ accounts for the switching period displacement. When $\Delta d = \Delta T_s = 0$, there is no i_{ind} current. Fig. 7 shows i_{ind} waveform over an utility period (T_u). The linear slope demonstrates the higher influence of Δd than ΔT_s. So the slope value can be approximated as $V_o \Delta d / L$.

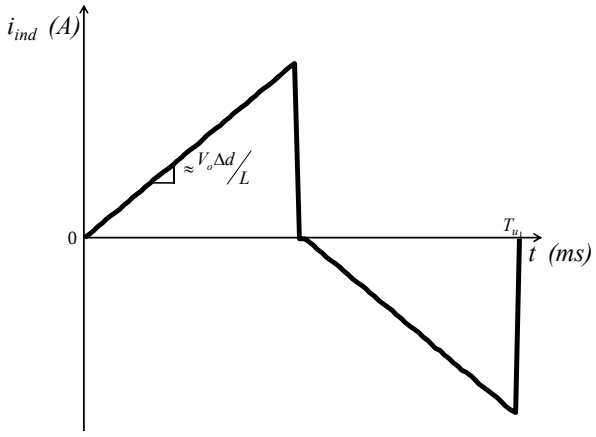


Figure 7. Current distortion created by the compensation errors waveform over an utility period

If a perfect power factor correction is achieved with an ideal compensation, the current demanded by the converter (i_{in_ideal}) can be written as:

$$i_{in\_ideal} = \sqrt{2}\,P_{in}/V_{in}\,sin(\omega t) \tag{9}$$

where P_{in} represents the demanded input power. But with a wrong compensation, the total input current will be the addition of this ideal current (i_{in_ideal}) and the current created by the compensation errors (i_{ind}):

$$i_{in} = i_{in\_ideal} + i_{ind} \tag{10}$$

Furthermore, the minim value of the inductor current is clamped to zero. For instance, with a value of $\Delta t_{on\text{-}off}$ = 10 ns and $\Delta t_{off\text{-}on}$ = 30 ns, T_s = 73.2 kHz, P_{in} = 640 W and V_{in} = 120 V_{rms}, 60 Hz, Fig. 8 shows the i_{ind} current and the ideal sinusoidal current, i_{in_ideal}, waveforms for this situation.

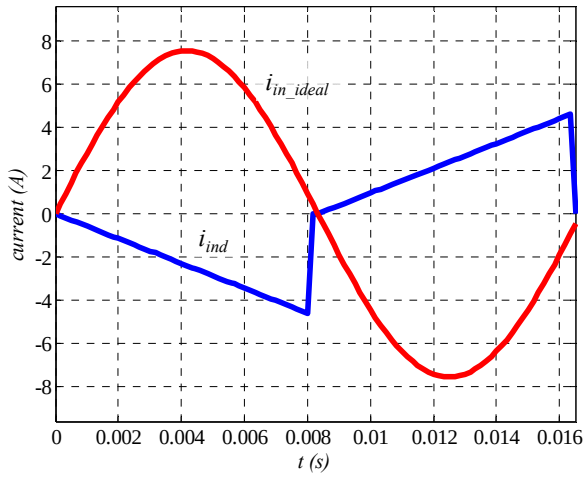


Figure 8. Ideal sinusoidal current (red) and current distortion (blue) waveforms

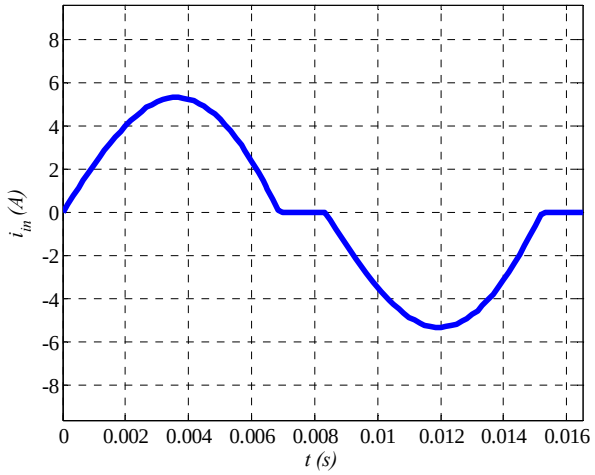


Figure 9. Total input current with $\Delta t_{on\text{-}off}$ = 10 ns and $\Delta t_{off\text{-}on}$ = 30 ns

Fig. 9 presents the input current waveform (i_{in}), addition of i_{ind} and i_{in_ideal} waveforms shown in Fig. 8. In this case, it can be seen a volt-second under-compensation accumulation across the inductor at the end of the half utility period.

IV. DRIVE SIGNAL'S DELAY DETECTION CIRCUIT

An auxiliary circuit is included in order to detect the instant when the inductor voltage transition due to the switch action occurs (v_{ds}). Then, the time difference between this event and the digital circuit switch command (*on/off* signal), generated by the algorithm NLC control, is measured with a resolution that depends on the clock frequency of the digital device (10 ns in this case). A diagram of the circuit is shown in the Fig. 10.

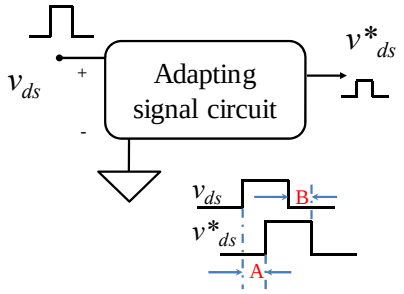


Figure 10. Diagram of the circuit implemented to detect the real inductor voltage transition

In this adapting circuit, a voltage divider and a level shifter adapts the MOSFET drain-to-source voltage level, a diode prevents negative voltage values. The laboratory test circuit includes an isolator. The result is a new digital input to the digital circuit, v^*_{ds} , as is shown in Fig. 10, from which the delay with respect the *on/off* output signal (Fig. 5) is obtained. It should be noted that v^*_{ds} is also delayed with respect v_{ds} because of the adapting signal circuit and its layout (see *A* y *B* in Fig. 10). As consequence, the drive signal's measured delays are $Del_{on\text{-}off}$ + *A* for the on to off transition, and $Del_{off\text{-}on}$ + *B* for the off to on transition. In order to obtain the real drive signal's delays, *A* and *B* values have to be substracted from the measured delays.

V. APPLICATION FOR HID LAMPS ELECTRONICS BALLAST

As proof of practical application, a prototype of the resulting PFC stage has been used to supply electronic ballasts for HID lamps. A system block diagram is shown in Fig. 11. Furthermore, taking advantage of digital circuit's capabilities, a voltage controller with two different gains has been implemented in order to eliminate unpleasant light flickering in the lamp. The first one has a slow dynamic response in order to achieve the power factor correction, and is applied for steady state condition. The second one provides a fast dynamic response to reject the utility fluctuations and to eliminate the light flickering. Fluctuation frequency has been set close to the maximum human eye flicker perception, i.e. 10 Hz.

It has been observed that HID lamps are sensitive to the supply voltage fluctuations. Here the cut-off frequency of the PFC voltage loop is extended in presence of utility disturbances taking into account the frequency range of the sensitivity curve defined by the IEC 61000-4-15. As a result, the light flickering perception is reduced without using a large PFC output capacitor. The fast dynamic response of the PFC voltage loop distorts the utility current, but this response is acceptable under utility transients. PFC voltage loop bandwidth is reduced when the utility returns to the steady-state condition, resulting in an adaptive PFC outer loop controller.

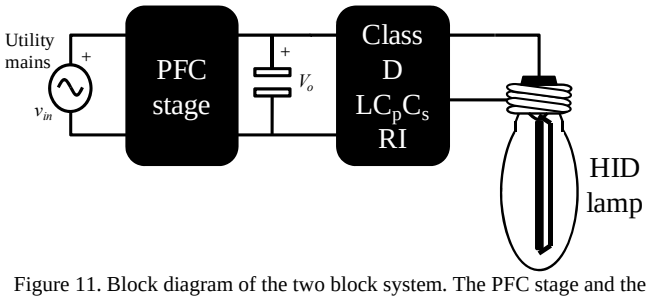


Figure 11. Block diagram of the two block system. The PFC stage and the electronic ballast.

The PFC stage is a boost converter (Fig. 1), and the electronic ballast is a class D LC_pC_s resonant inverter (RI). The output capacitor of the PFC stage is shown out of the boost converter to highlight that a reduced capacitance value has been used (68 μF) considering V_o ripple specifications and not hold-up time constrains.

A half-bridge resonant inverter is used for this application. This inverter achieves the required ballast action at reduced cost. This solution has been extensively reported in the literature [11]. A scheme of the resonant inverter is shown in Fig. 12.

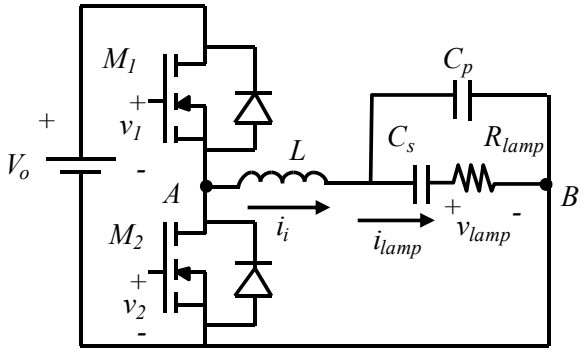


Figure 12. Class D LC_pC_s resonant inverter

VI. Experimental Results

The implemented boost converter has been designed for power conversion rate up to 1 kW and output voltage V = 400V. The inductor has been built with a soft saturation *Kool Mu* core with 115 turns resulting in an inductance L = 1.02 mH at 3 A. Soft saturation cores extend the CCM over a higher load range than the hard saturation counterparts. Switches are: power diode RHRP860 and MOSFET IRFP27N60K. The digital device is a Xilinx Spartan 3E family XC3S500E FPGA that is connected to the computer with a USB connector to observe internal signals.

In order to protect this digital device an optocoupled driver, HCPL-3120 and a magnetic isolator, IL712 have been used in the laboratory prototype. A schematic of the boost converter prototype is shown in Fig. 13.

To demonstrate the effective detection of the DCM, the load has been set at 160 W with V_{in} = 230 V_{rms} where DCM is approximately takes place over half the utility period.

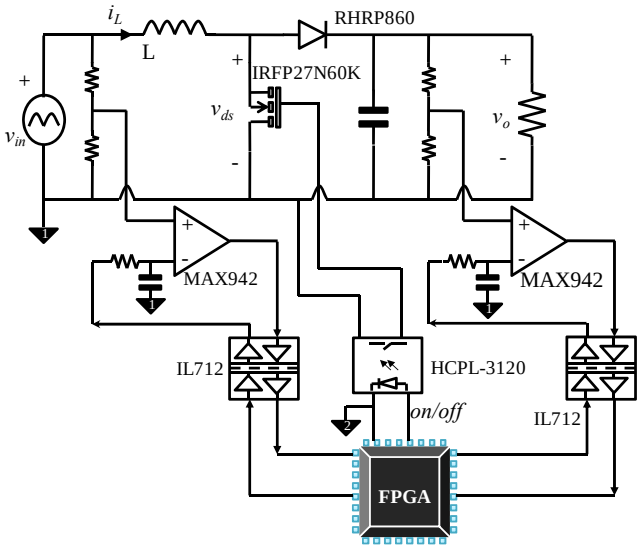


Figure 13. Boost converter prototype schematic.

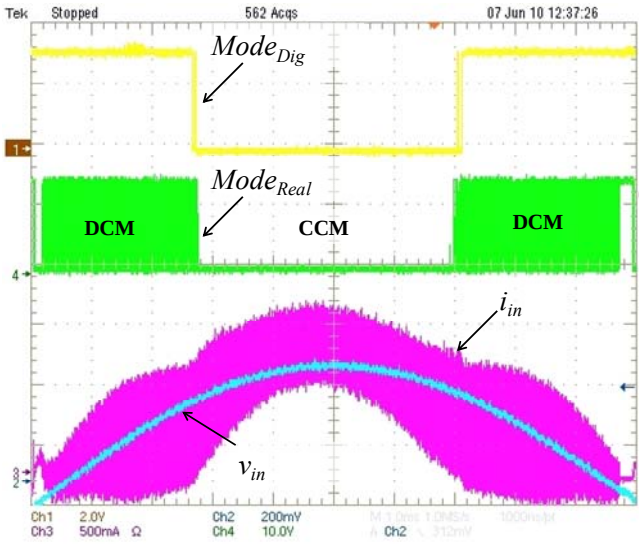


Figure 14. Input voltage and current over a half utility period with DCM and CCM situations.

Fig. 14 shows the input voltage and current waveforms over an utility semi cycle. The signal $Mode_{Dig}$ obtained from the current estimation process is compared against $Mode_{Real}$; a signal obtained from a current sensor, that detects zero input current, being "1" when in DCM, the input current is zero. Fig. 14 also shows the effect of the NLC algorithm for CCM when the converter operates in DCM.

Small volt-second estimation errors in each switching cycle accumulated over the utility period may increase the error in estimating the instant when the transition from DCM to CCM and vice versa occurs with $Mode_{Dig}$ resulting in large current distortion.

The circuit that detects the real inductor voltage transition includes a MC1450BCP level shifter, with an IL712 isolator

too. *A* and *B* delays, defined in Fig. 10, have been experimentally obtained and compensated with constants values in the NLC algorithm.

Fig. 15 shows the values of the switching delays defined in Fig. 5 over half the utility period under V_{in} = 230 V_{rms}, V_o = 400 V and P = 640 W At the beginning and at the end of the half utility period, the values of $Del_{on\text{-}off}$ increase. This occurs because the duty cycle is high, and then v_{ds} is high for a very short time, that is filtered in the analog circuit, and does not appear in v_{ds}^*. A maximum and minimum $Del_{on\text{-}off}$ = 550 ns and 450 ns has been set, respectively, in order to prevent the effect of false delay compensation.

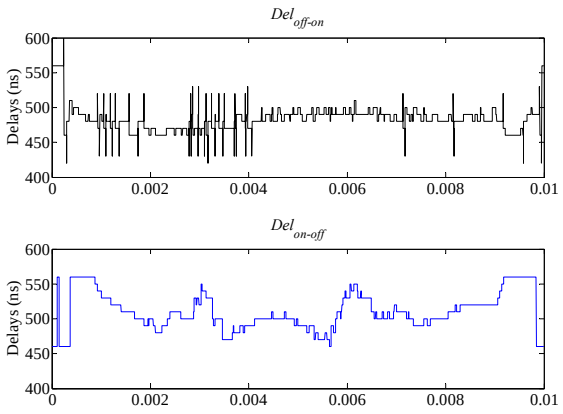
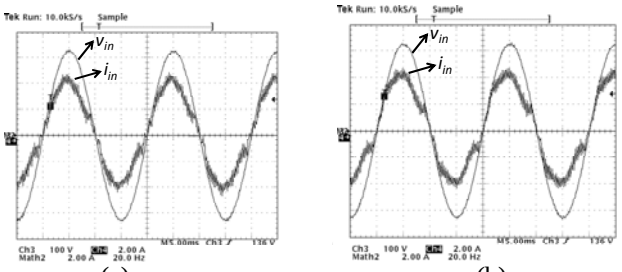


Figure 15. Measured delays

Fig. 16, Fig. 17 and Fig. 18 show experimental results that prove the improvement of the current shape when the autotuning algorithm is applied under an input voltage change (230 V_{rms} down to 220 V_{rms}, and then down to 200 V_{rms}). The power factor values are shown in Table I. Fig. 16 shows the initial situation (V_{in} = 230 V_{rms}), where power factor values are 0.994 (Fig. 16.a) with the autotuning algorithm and 0.989 without it (Fig. 16.b). Manually preset values are implemented to achieve the best results in the non-autotuning algorithm with V_{in} = 230 V_{rms}. Fig. 17 shows the current shape when a 10 V_{rms} step down input voltage is applied. Power factor values are 0.995 (Fig. 17.a) with the autotuning algorithm and 0.954 without it (Fig. 17.b). After that, a 20 V_{rms} step down input voltage is applied. With V_{in} = 200 V_{rms} a value of 0.992 (Fig. 18.a) with the autotuning algorithm and 0.885 without it (Fig. 18.b).

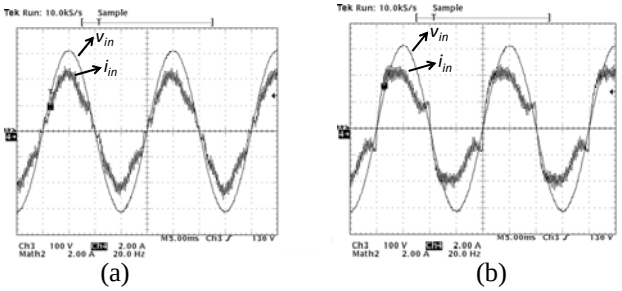
TABLE I. POWER FACTOR VALUES

v_{in}	***Autotuning algorithm***	***Without autotuning algorithm***	***Figure***
230 V_{rms}	0.994	0.989	Fig. 16
220 V_{rms}	0.995	0.954	Fig. 17
200 V_{rms}	0.992	0.885	Fig. 18



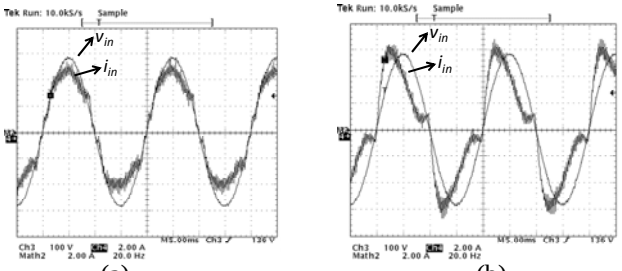
(a) (b)

Figure 16. Experimental results V_{in} = 230 Vrms, 50Hz, V_o = 400 Vdc P_{out} = 640 W, with Ch3 input voltage, Ch4 input current. a) Autotuning system (b): Non-autotunning system.



(a) (b)

Figure 17. Experimental results V_{in} = 220 Vrms, 50Hz, V_o = 400 Vdc P_{out} = 640 W, with Ch3 input voltage, Ch4 input current. a) Autotuning system (b): Non-autotunning system.



(a) (b)

Figure 18. Experimental results V_{in} = 200 Vrms, 50Hz, V_o = 400 Vdc P_{out} = 640 W, with Ch3 input voltage, Ch4 input current. a) Autotuning system (b): Non-autotunning system.

In the Electronic ballast application described in section V, the PFC stage works with V_{in} = 230 V_{rms}, 50 Hz, and V_o = 420 V_{dc} for a 150 W HID lamp. During the warm-up time, the input current is low and the power factor value is 0.99. Fig. 19 shows the steady state input current in the PFC stage. Lamp power is 150 W. The power factor has a value of 0.983. In this situation, a reduced bandwidth outer loop is implemented. The phase margin and the crossover frequency are 69º and 0.75 Hz, respectively.

After this, a 10 % fluctuation (230 V_{rms} – 207 V_{rms}) in the utility voltage is applied with 10 Hz frequency. Fig. 20 shows the current envelope with the two different implemented controllers, in order to evaluate the lamp current amplitude variation.

With the reduced bandwidth outer loop, utility fluctuation is not rejected. A lamp current variation appears, and therefore,

an unpleasant light flickering. Fig. 20 (a) shows this amplitude variation in the lamp. A power factor of 0.93 is measured.

In order to remove this light flickering, another outer loop with a wide bandwidth is applied. Now, the phase margin is 77º and the crossover frequency is 137 Hz. Fig 20 (b) shows the amplitude lamp variation current under the presence of fluctuations in the utility voltage when this outer loop is applied. Imperceptible light flickering is achieved now.

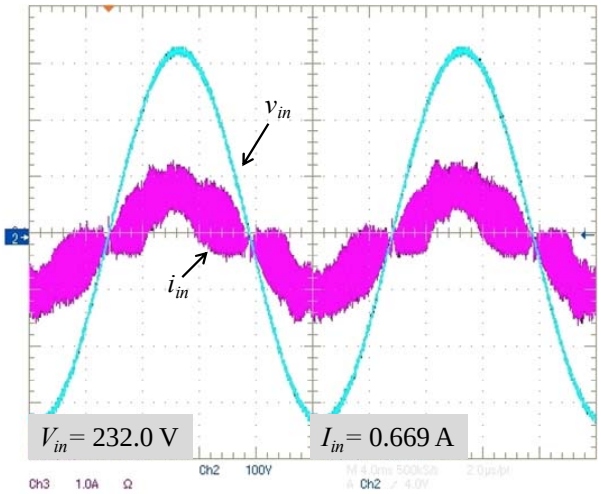
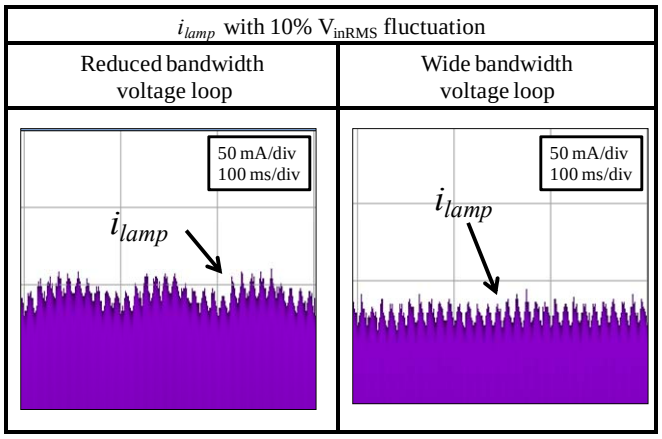


Figure 19. PFC stage waveforms under steady-state conditions. V_{in}=230V_{rms}, 50 Hz. Ch2 input voltage, 100 V/div, Ch3 input current, 1 A/div.



(a) (b)

Figure 20. Lamp current (i_{lamp}) under 10% V_{inRMS} fluctuation: (a) with a reduced voltage loop bandwidth and (b) with a wide bandwidth. V_{in} = 230 V_{rms}, ΔV = 10%, 50Hz, V_o = 420 Vdc, Pout = 150 W and 68 µF output capacitor.

Fig. 21 shows the PFC stage input current and the input voltage waveforms during utility fluctuation, with the wide bandwidth outer loop. The value of the power factor is 0.92. The input current is distorted because of the fast dynamic response, but this current is acceptable under utility transients.

After this utility fluctuation conditions, the first outer loop is applied again and the power factor correction returns to 0.983, as shown in Fig. 19.

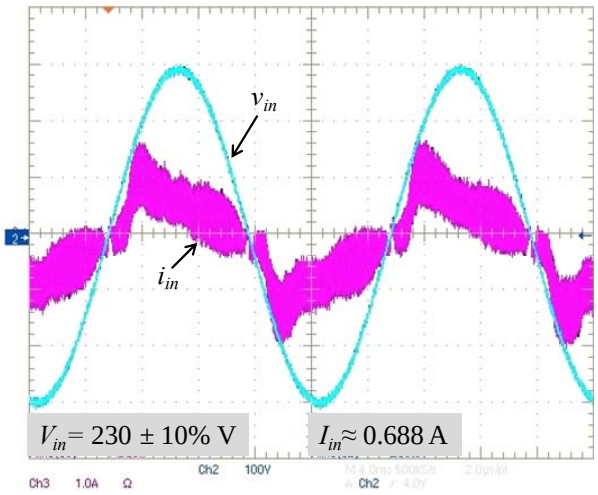


Figure 21. PFC stage waveforms under 10 Hz utility voltage fluctuations. V_{in}=230 ±10%V_{rms}, 50 Hz. Ch2 input voltage, 100 V/div, Ch3 input current, 1 A/div.

VII. CONCLUSIONS

An auxiliary circuit to measure the drive signal's delays in a sensorless power factor correction controller implemented in a digital device is presented. Instead of being measured, the input current is digitally rebuilt according to the finite-difference equations that define it. The input current value is a function of the input and output voltage values in the boost converter; which is the converter type of the presented prototype converter. The detection of the DCM operation increases the correspondence between the estimated and the actual input current in the PFC. Using the digitally rebuilt current, the real input current is controlled by a peak nonlinear-carrier control. Drive signal's delays cause an error between the real current and the digitally rebuilt current. The measured power factor under input voltage and load changes proves that the delay measurement and its dynamic (autotuning) compensation produces significant power factor improvement in comparison with the use of constant (non - autotuning) compensation.

A PFC sensorless boost prototype is used to supply a HID lamps electronic ballast. HID lamps are sensitive to the supply voltage fluctuations, and an unpleasant light flickering occurs when the fluctuation frequency is set close to the maximum human eye flicker perception. A voltage controller with two different outer loop bandwidths is designed for the PFC stage in order to reject utility voltage fluctuations without using a large PFC output capacitor. A reduced bandwidth loop is applied in steady state condition. During utility voltage fluctuations, an extended bandwidth loop is applied, removing the light fluctuations.

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