Current error compensation for current-sensorless power factor corrector stage in continuous conduction mode

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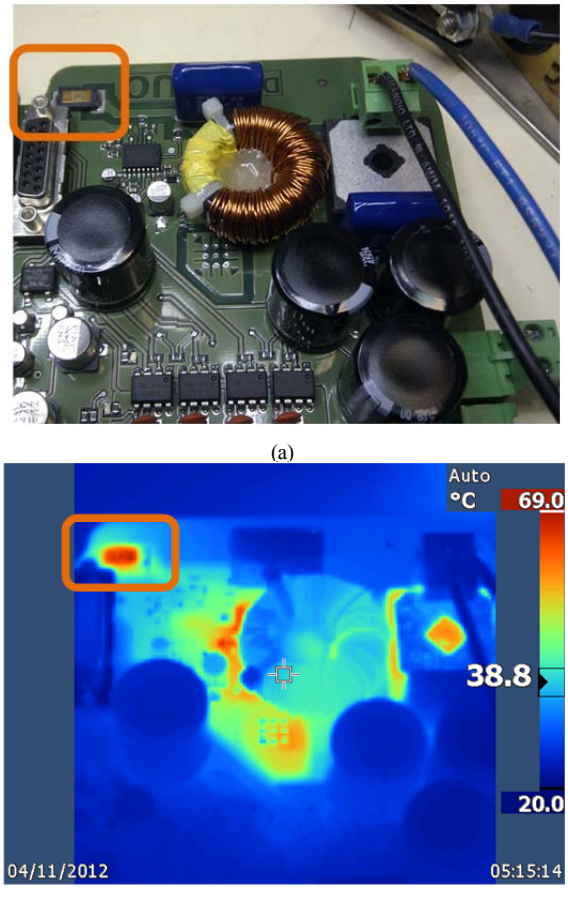
Abstract—**An universal digital PFC current-sensorless controller based on the control of the estimated current is presented. Parasitic elements cause a small difference between the measured input voltage and the voltage across the inductance in a boost converter, which must be taken into account to estimate the input current in a sensorless PFC digital controller. The article proposes a digital feedback control that cancels the time difference between DCM operation time of the real input current (T^{in}_{DCM}) and the estimated current (T^{reb}_{DCM}) to compensate for the deviation caused by the parasitic elements, and so minimize the current estimation error. Experimental results, obtained using a boost PFC converter under different conditions, are shown for verification purposes**

Keywords- Digital control, power factor correction, sensorless control, digital error compensation, feedback loop, universal PFC controller.

I. INTRODUCTION

Since the complexity of analog-to-digital conversion (ADC) of the current is greater than in the case of the voltage conversion, current sampling in digitally-controlled high-frequency switched-mode power supplies is an issue that has received many authors' attention. A resistive sensor is the most adopted solution for current sampling. The power dissipated by this resistor causes a hot spot in the converter, as is shown in Fig. 1. The first criteria in determining the resistor's value is often the gain of the amplifier stage (Fig. 2) [1]. Furthermore, the current ADC must have a high bandwidth, increasing the cost in comparison with the voltage ADCs. Focused on proposing cost-effective solutions without losing performance, current estimation techniques based on voltage measurements are presented in [2-4] and [5] for single-phase and multiphase converter applications respectively. For PFC applications, approaches like [6-13] propose the elimination of the traditionally required analog-to-digital conversions. Different authors have presented approaches for Boost sensorless PFC controllers [10-13] where parasitic elements are measured and taken into account in the controller to compensate for their effects. This work is based on [6, 7] where the input rebuilding concept is used. The variable volt-seconds (vs_L) across the inductance is estimated in each switching period, and a small error (current estimation error) per switching period accumulated over the half line cycle, causes current distortion. The aim of this paper is to study the influence of the parasitic elements and proposes a feedback control to compensate for the unmeasured volt-second estimation error.

This paper is organized as follows. The influence of the parasitic elements in a PFC boost converter with current rebuilding controller [6, 7] is studied in Section II. Section III discuses the compensation of this parasitic elements. Section IV presents an auxiliary circuit for the DCM detection that is



(a)

(b)

Figure 1. (a) PFC converter with current sensor. (b) Thermal image at full load.

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used in a new feedback correction of the estimation error, presented in Section V. Experimental results are presented in Section VI for a 1 kW Boost converter under different input voltage and power load, finalizing with conclusions.

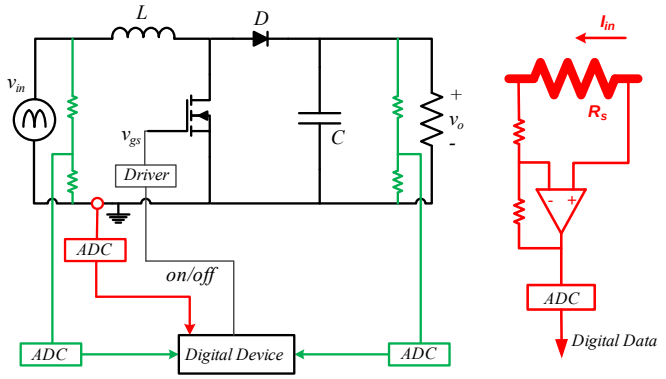


Figure 2. (a) Typical PFC scheme with digital control with current sensor. (b) Analog to digital conversion circuit of the input current.

II. INFLUENCE OF THE PARASITIC ELEMENTS IN CURRENT ESTIMATION

Nonlinear-carrier (NLC) control technique [14] is used in this digital controller. The carrier signal and the variable estimated, the (rebuilt) input current i_{inreb}, are compared to define the duty cycle in each switching period. The average rebuilt current in each switching period follows the input voltage. The current estimation error due to drive signal's delay effect is analyzed in [6] and a feed-forward compensation is presented in [7] for a Boost converter. Figure 3 shows the diagram of a boost converter with the most relevant parasitic elements whose effect is not taken into account in the feed-forward compensation.

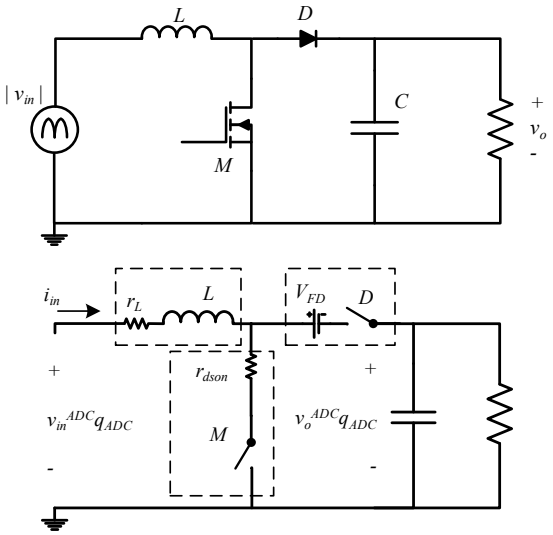


Figure 3. Top: Boost converter. (b) Boost converter diagram with parasitic elements

The digital input and output voltages, v_{in}^{adc} and v_o^{adc}, are used to estimate the input current. According to Fig. 3 and considering the ADC conversion bin, q_{ADC}, ideally identical for the input and output voltages (q_{ADC}=1 V/bit), the expressions that define inductor current (i_{in}) variation during ON (Δi_{on}) and OFF (Δi_{off}) state are (1) and (2), respectively.

$$\Delta i_{on} = \frac{v_{in}^{adc} - r_L i_{in} - r_{dson} i_{in}}{L} dT_{sw} \quad (1)$$

$$\Delta i_{off} = \frac{v_{in}^{adc} - r_L i_{in} - V_{FD} - v_o^{adc}}{L} (1-d) dT_{sw} \quad , \quad (2)$$

where r_L is the equivalent series resistor of the inductor, V_{FD} is the diode conduction voltage, r_{dson} is the on-state MOSFET resistor, d represents the duty cycle and T_{sw} the switching period. The average voltage drop in the parasitic elements in each switching period T_{sw}, is:

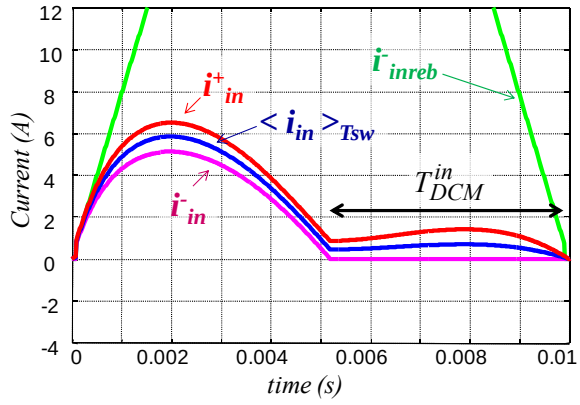
$$\langle v_{par} \rangle_{T_{sw}} = -r_L i_{in} - r_{dson} i_{in} d - V_{FD}(1-d), \quad (3)$$

The duty cycle command in the NLC control is given by $d = 1 - v_{in}/v_o$, so (3) can be rewritten as:

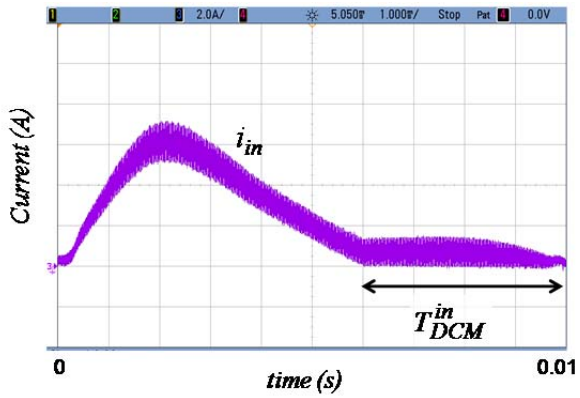
$$\langle v_{par} \rangle_{T_{sw}} = -r_L i_{in} - r_{dson} i_{in} \left(1 - \frac{v_{in}}{v_o}\right) - V_{FD} \frac{v_{in}}{v_o} =$$

$$= -\left[\left(r_L + r_{dson} - r_{dson} \frac{v_{in}}{V_o}\right) \frac{P_{IN}}{V_{IN}^2} + \frac{V_{FD}}{V_o}\right] v_{in} \, , \quad (4)$$

being V_{IN} the rms input voltage, P_{IN} the average input power over the utility period, and neglecting the output voltage ripple ($v_o = V_o$). To simplify the analysis only the effect of r_L is considered, because for a boost converter r_L is the parasitic element which affects in the whole switching period (r_{dson} only during ON time and V_{FD} in the OFF time). Therefore, the average parasitic voltage drop in each switching period T_{sw} can



(a)



(b)

Figure 4. Current waveforms (a) simulated current waveform. (b) Experimental current waveforms illustrating the operation of the sensorless Boost PFC without compensation of the parasitic elements.

be approximated as:

$$\langle v_{par} \rangle_{T_{sw}} \cong -\left[r_L \frac{P_{IN}}{V_{IN}^2} \right] v_{in} \quad (5)$$

The volt-second deviations caused by the parasitic elements depend on the components/devices used in the converter, the temperature, the switching frequency, etc; which in turn varies with the power (P_{IN}).

Input rebuilding concept is presented in [6] and [7]. Neglecting the influence of parasitic elements, (6) and (7) are the equations implemented in the digital device to estimate de input current.

$$\Delta i_{inreb,on} = \frac{v_{in}^{adc}}{L} dT_{sw} \quad (6)$$

$$\Delta i_{inreb,off} = \frac{v_{in}^{adc} - v_o^{adc}}{L} (1-d) dT_{sw}, \quad (7)$$

It can be observed that the average voltage across the inductor from (1) and (2) $<v_{par}>_{Tsw}$, is lower than the estimated in (6) and (7). This small error is accumulated in each switching period over the half-line cycle resulting in low power factor. Since i_{in} is lower than the estimated i_{inreb}, the voltage loop increases i_{in} and i_{inreb} to assure the expected output power. Figure 4.a analyzes the cases where the estimated volt-seconds across the inductor are lower than the actual ones due to non-compensated parasitic effects. The variables i^+_{in}, i^-_{in}, and $<i_{in}>_{Tsw}$ represent the peak, valley and average values of i_{in} in each switching period, respectively; while i^-_{inreb} represents the estimated valley value of the input current calculated in each switching period. The estimation error is accumulated throughout the utility period. Fig. 4.b shows the correspondence between the simulated and measured input currents. In this situation, it can be observed that i_{in} operates in DCM longer than i_{inreb}.

III. Digital Compensation of the Parasitic Effects

To compensate the volt-seconds estimation error, the proposed control introduces a digital signal v_{dig} to modify the estimated voltage drop in the inductor. Two alternatives are analyzed in this work. The first one decreases v_{in}^{adc} and the second one increases v_o^{adc}.

A. Modifying the input voltage value, v_{in}^{adc}

With v_{dig} signal, the digital value that emulates the input voltage v_{in}^{adc} is decreased, resulting in v_{in}^{adc*} that is used to rebuild the input current in equations (6) and (7), substituting v_{in}^{adc} by v_{in}^{adc*}, and v_o^{adc} is not modified

$$v_{in}^{adc*} = v_{in}^{adc} - v_{dig} \quad (8)$$

The value of v_{dig} that compensates the parasitic elements effects is obtained from (5)

$$v_{dig} = \left[r_L \frac{P_{IN}}{V_{IN}^2} \right] v_{in} \quad (9)$$

With this option, v_{dig} has to be a proportional to the input voltage, v_{in}. Assuming a pure sinusoidal input voltage $v_{in} = \sqrt{2} V_{IN} sin(\omega t)$, total parasitic elements effect is compensated if the digital control introduces a digital signal $v_{dig} = V_{dig} sin(\omega t)$ whose amplitude, V_{dig} is given by (10).

$$V_{dig} = \left[r_L \frac{P_{IN}}{V_{IN}^2} \right] \sqrt{2} V_{in} \quad (10)$$

This proposal includes the case in which v_{in}^{adc*} is fully synthesized by the digital circuit and its amplitude is controlled to compensate the effect of the parasitic elements.

B. Modifying the output voltage value, v_o^{adc}

In this second option, the digital value that emulates the output voltage v_o^{adc} is increased, resulting in v_o^{adc*} that is used to rebuilt the input current in equations (6) and (7), and v_{in}^{adc} is not modified.

$$v_o^{adc*} = v_o^{adc} + v_{dig} \quad (11)$$

The average compensation voltage v_{dig}, in each switching period T_{sw}, is given by (12) for the PFC boost converter operating in (CCM) with NLC control, $d = 1 - v_{in}/v_o$:

$$\langle v_{dig} \rangle_{T_{sw}} = -v_{dig}(1-d) = -v_{dig} \frac{v_{in}}{V_o} \quad (12)$$

The value of v_{dig} that compensates the parasitic elements effects is obtained comparing (5) and (12):

$$v_{dig} = \frac{V_o r_L P_{IN}}{V_{IN}^2} \quad (13)$$

With this alternative, parasitic elements effect can be compensated with a constant value ($v_{dig}=V_{dig}$). In comparison with the first alternative, this compensation is not dependent on the input voltage waveform and therefore is robust in presence of input voltage distortion. Furthermore, no zero crossing detector circuit and phase-locked loop are needed, so the complexity of the control algorithm is lower. Due to that, this second option is the implemented in the digital controller. Figures 5 and 6 show the current waveforms under input voltage distortion with a *THDv=5%* for both alternatives. The behavior of the first alternative is shown in Fig. 5. Current estimation error; i_{in}^{error} represents the difference between the valley value of i_{in} in each switching period (i^-_{in}), and i^-_{inreb} (valley value of the calculated input current in each switching period). Current waveforms modifying the output voltage value are presented in Fig. 6

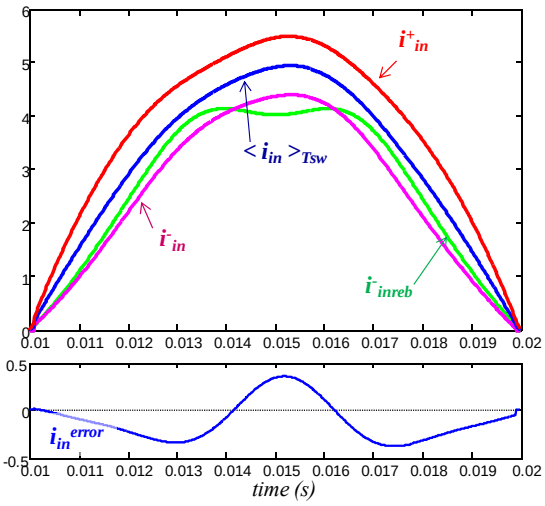


Figure 5. Current waveforms over a half-line cycle modifying the input voltage value. Top: Simulated current waveforms for the real and rebuilt input currents.. Bottom: Current estimation error.

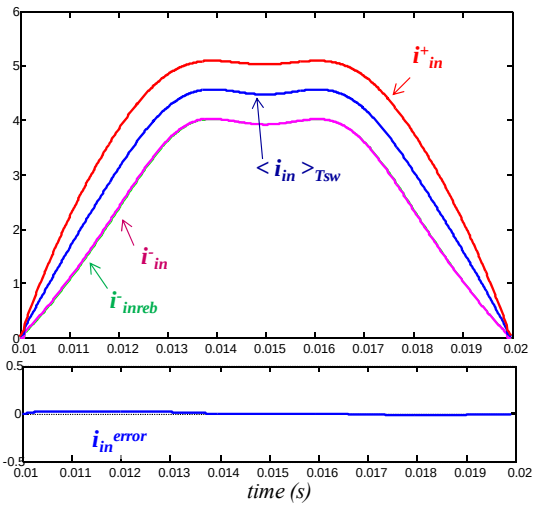


Figure 6. Current waveforms over a half-line cycle modifying the output voltage value. Top: Simulated current waveforms for the real and rebuilt input currents.. Bottom: Current estimation error.

IV. Discontinuous Conduction Auxiliary Detection Circuit

As it has been shown in Fig. 4, the time in which discontinuous conduction mode (DCM) occurs is a parameter that enables the detection of discrepancy between i_{inreb} and i_{in} . In the case shown in Fig. 2, this time is T^{in}_{DCM} for i_{in}, while it is nearly zero for i_{inreb}.

An auxiliary circuit that is capable of determining the converter mode of operation (CCM o DCM) is presented in this work. Figure 7 shows the hardware architecture (Fig. 7a) and the circuit behavior (Fig. 7b). A digital signal $DCMi_{in}$, indicates the converter operating mode by its logic level (e.g., $DCMi_{in}$ = '0' for CCM operation and $DCMi_{in}$ = '1' for DCM operation). This circuit, similar to the one described in [15] and [16], compares the output voltage v_o, with the MOSFET drain-to-source voltage v_{ds}, adapted with two equal resistor dividers ($R_{ds1} = R_{o1}$, $R_{ds2} = R_{o2}$), with an analog comparator. In CCM operation $v_{ds} = v_o + V_{FD}$, (V_{FD} is around 2 V and $v_o \approx 400\ V$) during the whole OFF time, but this is not true in DCM operation. Assuming that both MOSFET and power diode are ideal, drain-to-source voltage v_{ds} adopts the value of input voltage as soon as input current i_{in} reaches zero. But the inherited parasitic elements of the power switches cause oscillations in the drain-to-source voltage around v_{in} **[17].**

The comparator output signal x_1, is registered at the beginning of the switching period using the *on/off* signal rising edge, that is internally available in the digital device. If x_1 is high at this sample instant, the boost converter is operating in DCM ($DCMi_{in}$ = '1'). Conversely, if sampled x_1 is low, the converter is operating in CCM ($DCMi_{in}$ = '0').

In the case of the digitally rebuilt input current i_{inreb}, a signal indicates if i_{inreb}=0 at the beginning of the switching period (DCM operation is estimated and $DCMi_{inreb}$ = *'1'*) or not (CCM operation is estimated and $DCMi_{inreb}$ = *'0'*) as is presented in [7].

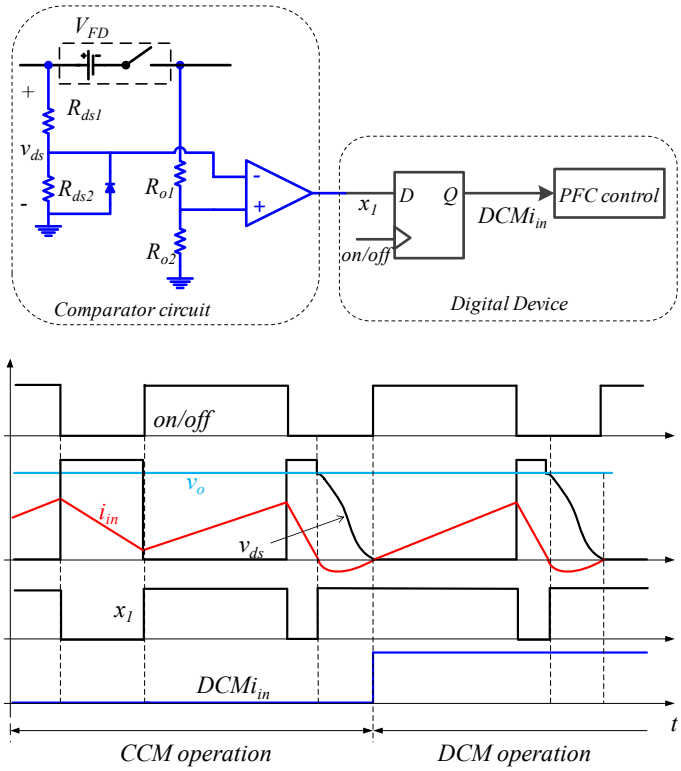
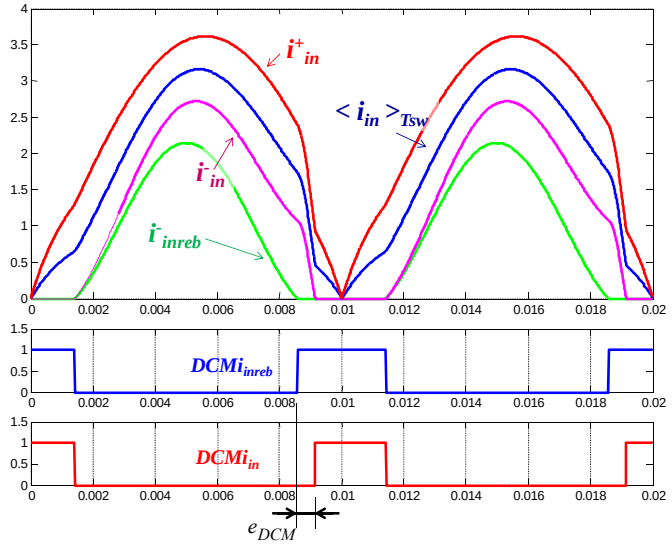


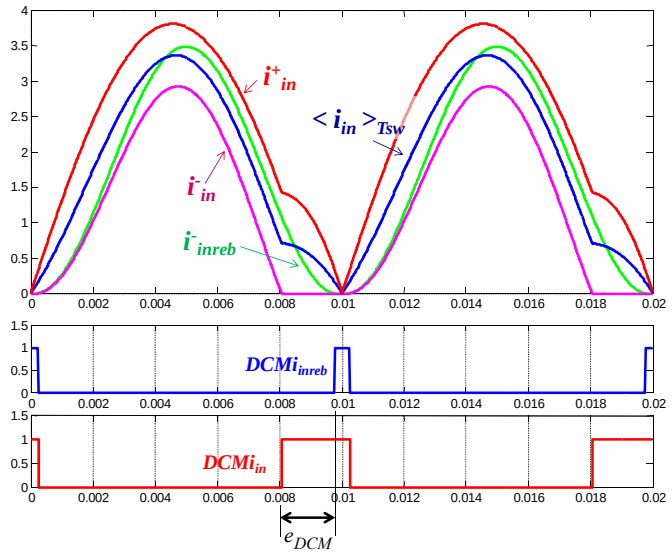
Figure 7. DCM condition detection auxiliary circuit for the real input current. Top: Hardware architecture. Bottom: Circuit waveforms.

V. Feedback Compensation of the Discontinuous Conduction Mode Time Discrepancy

The previous works [10-13], which also avoid the input current measurement, propose a PFC digital control that includes the measurement of the parasitic elements (r_L, V_{FD}, r_{dson}) and applies a duty cycle command d, according to these elements. But parasitic elements influence change with the temperature, frequency and the components used in the PFC converter. Discontinuous conduction mode (DCM) appears near the input line zero crossings and the time difference between the $DCMi_{in}$ and $DCMi_{inreb}$ events, e_{DCM}, is related to the current estimation error and the reduction of the power factor. Figure 8 shows the simulation waveforms for different values of V_{dig}. An overcompensation of the parasitic elements influence is presented in Fig. 8.a, where (14) is not fulfilled and $V_{dig} > V_{FD} + V_o r_L P_{IN}/V_{IN}^2$. In this case, $i_{inreb} < i_{in}$, over the half line cycle, so the output voltage is higher than the expected one and the voltage loop decreases i_{in} and i_{inreb} to set output voltage at the reference value. As a result, T^{in}_{DCM} is lower than T^{reb}_{DCM}. On the other hand, if $V_{dig} < V_{FD} + V_o r_L P_{IN}/V_{IN}^2$, the parasitic elements effect is not totally compensated. Due to that, $i_{inreb} > i_{in}$, over the half line cycle and T^{in}_{DCM} is higher than T^{reb}_{DCM}, as is presented in Fig. 8.b. The total compensation is achieved if (14) is fulfilled. This case is presented in Fig. 8.c, where the DCM times are matched, $T^{in}_{DCM} = T^{reb}_{DCM}$, and consequently the current estimation error is cancelled, $i_{in}^{error} \approx 0$.



(a)



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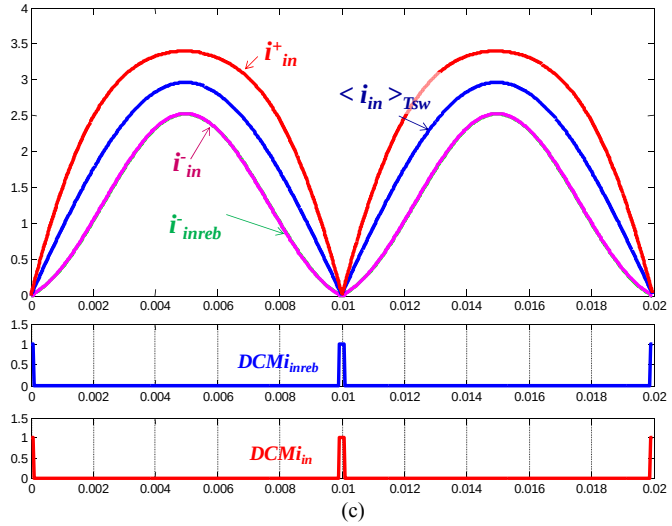

(c)

Figure 8. Simulation results for different values of V_{dig}. (a) Situation with volt-second overcompensation. (b) Situation with volt-second undercompensation. (c) Situation with correct volt-second compensation.

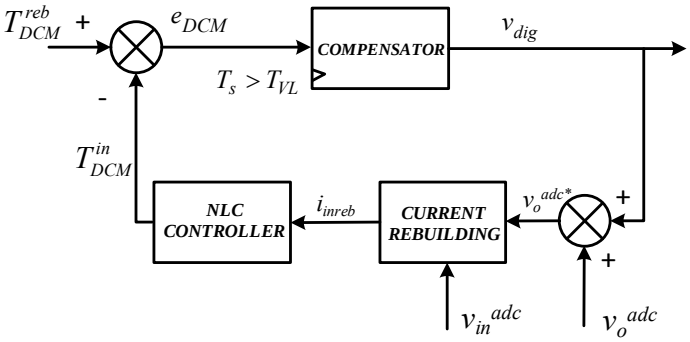

Figure 9. Block diagram of the proposed controller

To obtain a universal PFC controller that compensates any parasitic elements influence, the proposed control is a low frequency feedback loop that sets the value of the digital signal v_{dig}, presented in the Section III (modifying the output voltage digital value $v_o^{adc*} = v_o^{adc} + v_{dig}$) to compensate the parasitic elements effect up to the point where the difference between the DCM time of i_{in}, and i_{inreb}, ($T^{in}{}_{DCM}$) and ($T^{reb}{}_{DCM}$), respectively is cancelled. In the proposed controller, e_{DCM} is the input of the PI compensator, which adjusts the value of the signal v_{dig} until the DCM times matches, i.e. $e_{DCM}=0$. In this case, the current estimation error is eliminated, assuring a high power factor. The sample period of this PI compensator (T_s) is selected higher enough than the output voltage loop response (T_{VL}) to compensate for the difference between $T^{in}{}_{DCM}$ and $T^{reb}{}_{DCM}$ without interfering with the PFC outer loop. A block diagram of the proposed controller is shown in Fig. 9.

The compensation of the parasitic elements influence is presented in section III considering only r_L. Taking into account all parasitic elements (r_L, r_{dson} and V_{FD}), expression (13) can be rewritten as

$$v_{dig} = V_{FD} + \frac{V_o P_{IN}}{V_{IN}^2}\left[r_L + r_{dson}\left(1 - \frac{v_{in}}{V_o}\right)\right], \qquad (14)$$

The on-state MOSFET resistor r_{dson}, introduces a variable component in (14) over the half line cycle. The proposed DCM times error feedback loop tries to match DCM times with a constant digital signal $v_{dig}=V_{dig}$ despite not fulfilling (14) totally. Simulation results in steady-state operation are presented in Fig. 10 with parasitic elements values of $r_L = 0.3$ Ω, $V_{FD} = 2.1$ V and $r_{dson} = 0.5$ Ω for a power load of 640 W. The current estimation error i_{in}^{error}, over the half line cycle is shown in the graph located in the middle, and the harmonic content of i_{in}^{error} is presented at the bottom (in blue) with the IEC 61000-3-2 class C limits (in red) for these power load. All the current harmonics are caused due to i_{in}^{error}. Despite of using a constant value V_{dig} to compensate parasitic elements effect, it can be observed that the current harmonics limits are fulfilled and the simulated power factor value is 0.996.

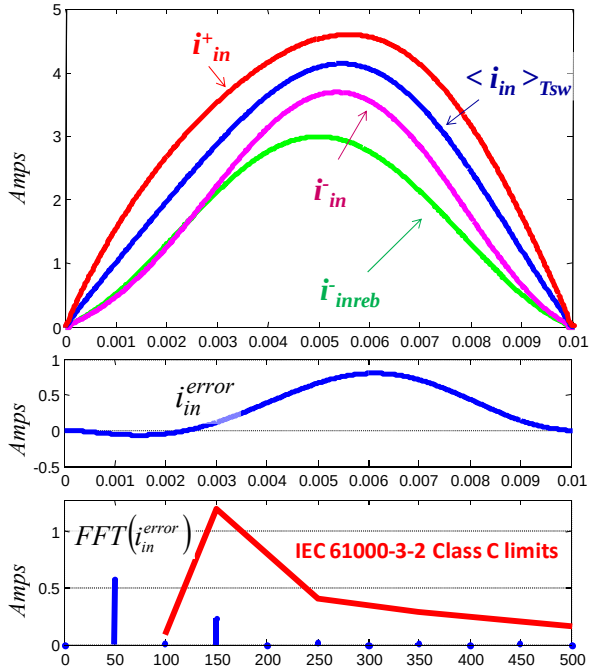

Figure 10. Simulation results with the proposed feedback loop with parasitic elements values of r_L = 0.3 Ω, V_{FD} = 2.1 V and r_{dson} = 0.5 Ω for a power load of 640 W. Top: Simulated current waveforms for the real and rebuilt input currents. Middle: Current estimation error. Bottom: FFT of the current estimation error waveform vs IEC 61000-3-2 limits.

VI. Experimental Results

A 1 kW boost converter with the proposed digital feedback loop has been built and tested. The circuit scheme that corresponds to the experimental prototype is shown in Fig. 11. The output voltage reference is 400 V_{dc} with an input voltage ranging from 85 V_{rms} to 250 V_{rms}. The switching frequency is 70 kHz. To demonstrate the universality of the controller with the feedback control, two different inductors have been built, and the results are achieved without modifying any parameter of the digital controller. The two inductors are shown in Fig. 12. The first inductor has been built with a RM12-3C90 core, resulting in inductance *L1= 1 mH* and r_{L1} = *0.25* Ω. The second inductor has been built with a soft saturation Kool mμ core 77071. In this case, the inductance *L2=1.5 mH and* r_{L2} = *0.35* Ω. The output capacitor *C = 220 uF*, the MOSFET and diode used to built the prototype were a IRFP27N60K from International Rectified ™ with r_{dson} = *0,18* Ω and a IDH12S60 from Infineon ™ with V_{FD} = 1.7 V. The digital PFC controller and the feedback loop were described in VHDL and implemented on a XC3S200E field programmable gate array (FPGA) of Xilinx. A second order *ad-hoc* sigma delta ADC is used for the output voltage and a commercial TLV1572 serial 10-bit ADC for the input voltage to obtain the voltage data. Figure 13 shows the main waveforms of the DCM condition detection circuit for the real input current with R_{ds1} = R_o = *1.2* MΩ and R_{ds2} = R_{o2} = *9.31* kΩ. The digital signal, $DCMi_{inreb}$ changes to '1' when the first DCM oscillation in the drain-to-source voltage occurs. It can be seen how experimental and theoretical waveforms (Fig. 7) are in good agreement.

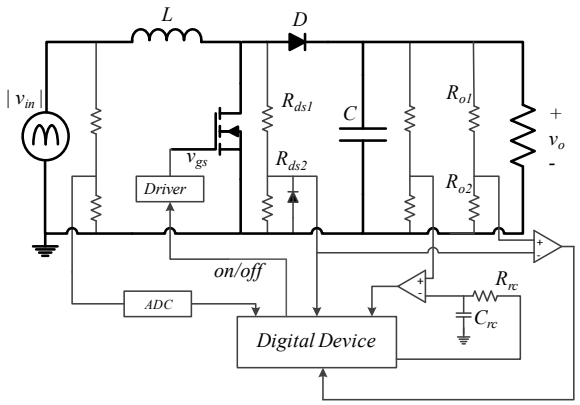

Figure 11. Circuit scheme of the proposed digital controller.

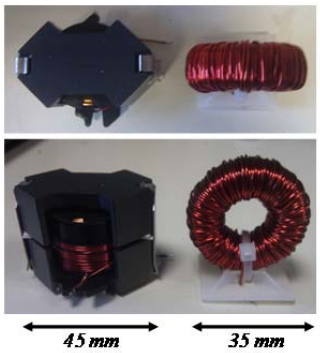

Figure 12. Inductors used in the experimental results, Left: *L1= 1 mH* (RM12-3C90 core, with r_{L1} = 0.25 Ω). Right: *L2= 1.5 mH* (soft saturation kool mu core 77071 with r_{L2} = 0.35 Ω)

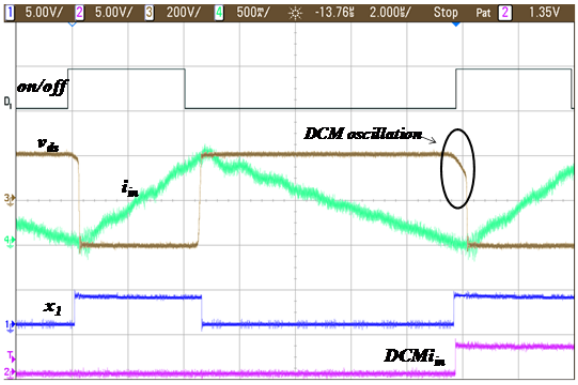

Figure 13. Experimental results for the DCM condition detection circuit for the real input current

The experimental results in the steady state operation are shown in Figs. 14-17 for different input voltages (85 V_{rms} – 60 Hz and 230 V_{rms} – 50 Hz), output power and both inductances (*L1* and *L2*). It can be observed that sinusoidal input current is achieved and DCM times are matched. Power factor and Total harmonic distortion of the input current (*THDi*) values are listed in Table I for wide input voltage (from 85 V_{rms} – 60 Hz to 230 V_{rms} – 50 Hz) and output power ranges.

Measured *THDi* values are a little higher with *L1* than with *L2*. This is caused by the current dependent inductance of the inductor built with a soft saturation core [18]. The aim of using

this inductance in the proposed controller is to show the behavior of the controller under two different conditions. The use of *L2* on one hand introduces a non-linear behavior that produces higher current distortion as the current increases and on the other hand keeps the CCM operation for a higher load range. Despite this aspect, the experimental results present high power factor values for all the tested conditions.

The behavior of the sensorless PFC boost controller under different distorted input voltage is shown in Fig. 18. The time evolution of the e_{DCM} value under a large load step down (970-640 W) is shown in Fig. 19. After the error peak value which occurs when the load step is applied, the fine feedback compensation modifies the V_{dig} amplitude, cancelling the DCM times error reaching a steady state condition with e_{DCM}=0 in around six seconds.

VII. Conclusion

An universal current sensorless controller for Boost PFC stages operating in CCM has been presented. Making the most of the digital control capabilities, the traditional current sensing analog circuit is substituted by a simpler circuit (two resistor dividers and a comparator) that detects DCM condition in the input current translating the pulsated drain-to-source voltage into a digital signal. With this circuit, an indirect measurement of the current distortion is obtained by comparing the actual and estimated DCM times.

The effect of the parasitic elements in the input current estimation for sensorless power factor correction Boost digital controllers operating in CCM has been analyzed. In this case, this current estimation is carried out by measuring the input, output and MOSFET drain-to-source voltages.

The error between the estimated and actual DCM periods close to the zero crossing of the input voltage is a key variable to accurately correct the error in the estimation of the input current and the consequent distortion. An auxiliary circuit detects DCM condition in the input current comparing drain-to-source voltage with the output voltage during OFF-time.

A new feedback loop generates a digital signal to compensate the parasitic elements influence, modifying the output voltage measurement used to estimate the input current, and minimizes this DCM time error. This feedback loop autotunes the value of the digital signal when the converter operates in a wide load or voltage range. With this feedback loop, parasitic element values do not need to be measured, and are compensated for automatically. The proposed current sensorless digital controller simplifies the design of PFC stages because it presents no dependence on its components.

Experimental results show a boost PFC converter under different load conditions achieving high power factor with a reliable performance.

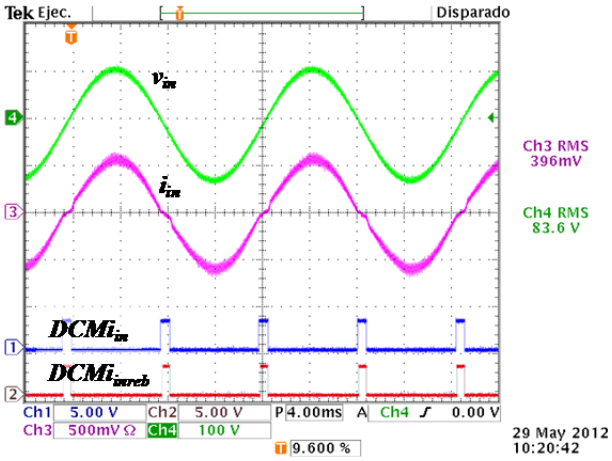

Figure 14. Converter waveforms. V_{IN} = 85 V_{rms} (60 Hz), P_{IN} = 320 W, V_o = 400 V_{dc}, *L1= 1 mH and* r_{L1} = 0.25 Ω

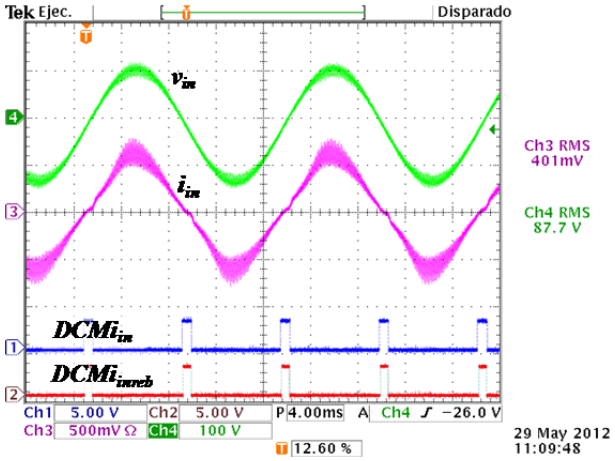

Figure 15. Converter waveforms. V_{IN} = 85 V_{rms} (60 Hz), P_{IN} = 320 W, V_o = 400 V_{dc}. *L2=1.5 mH and* r_{L2} = 0.35 Ω.

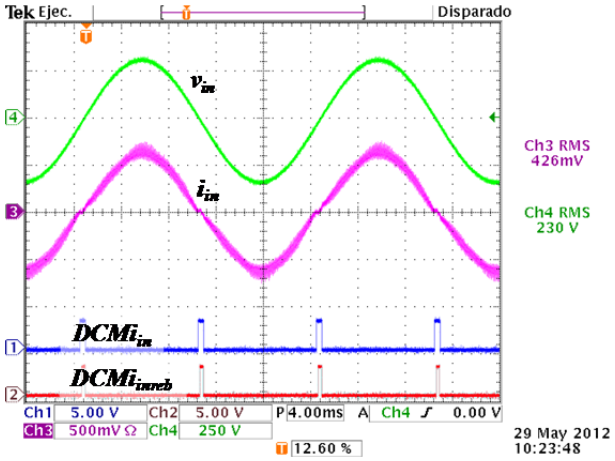

Figure 16. Converter waveforms. V_{IN} = 230 V_{rms} (50 Hz), P_{IN} = 970 W, V_o = 400 V_{dc}. *L1= 1 mH* and r_{L1} = 0.25 Ω

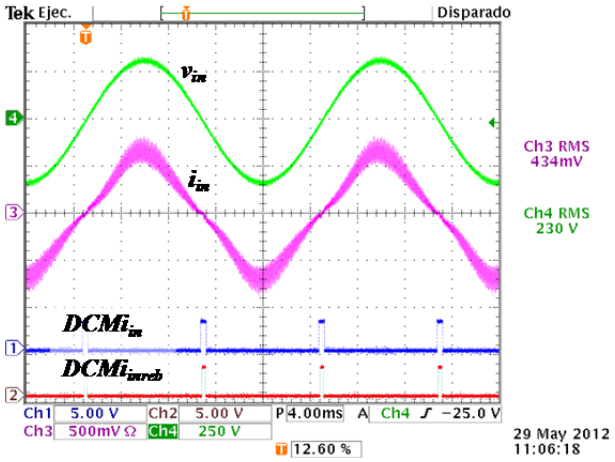

Figure 17. Converter waveforms. V_{IN} = 230 V_{rms} (50 Hz), P_{IN} = 970 W, V_o = 400 V_{dc}. *L2=1.5 mH and* r_{L2} = 0.35 Ω.

TABLE I.
POWER FACTOR AND THDI FOR DIFFERENT CONDITIONS

	L1 = 1 mH			*L2 = 1.5 mH*		
V_{in}	P_{IN}	PF	THDi	P_{IN}	PF	THDi
250 V_{rms}	970 W	**0.999**	5.6 %	970 W	**0.995**	10.5 %
	800 W	**0.998**	6.3 %	800 W	**0.996**	9.5 %
	645 W	**0.997**	6.8 %	645 W	**0.997**	8.5 %
	460 W	**0.993**	8.0 %	460 W	**0.994**	9.0 %
230 V_{rms}	975 W	**0.999**	4.6 %	970 W	**0.995**	10.5 %
	810 W	**0.998**	6.0 %	800 W	**0.995**	9.8 %
	650 W	**0.998**	6.0 %	640 W	**0.996**	9.1 %
	480 W	**0.998**	7.0 %	460 W	**0.997**	8.1 %
180 V_{rms}	825 W	**0.999**	4.8 %	820 W	**0.994**	10.5 %
	650 W	**0.999**	3.9 %	650 W	**0.996**	8.6 %
	485 W	**0.998**	5.0 %	485 W	**0.997**	7.1 %
	320 W	**0.997**	6.2 %	323 W	**0.998**	5.4 %
120 V_{rms}	495 W	**0.999**	4.1 %	497 W	**0.995**	9.8 %
	329 W	**0.998**	5.2 %	323 W	**0.995**	9.8 %
	158 W	**0.989**	12.8 %	159 W	**0.990**	10.0 %
85 V_{rms}	330 W	**0.999**	3.9 %	161 W	**0.998**	5.0 %
	161 W	**0.998**	5.3 %	336 W	**0.996**	9.0 %

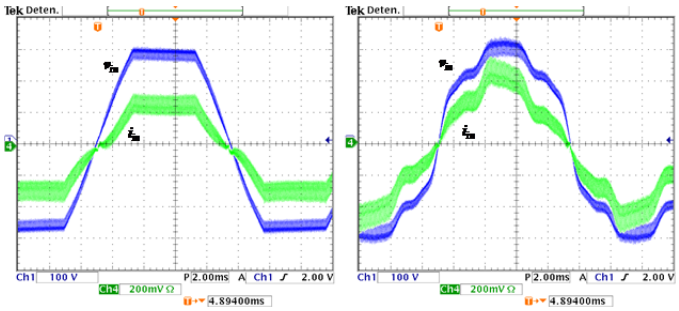

Fig. 18. Experimental results with input voltage distortion

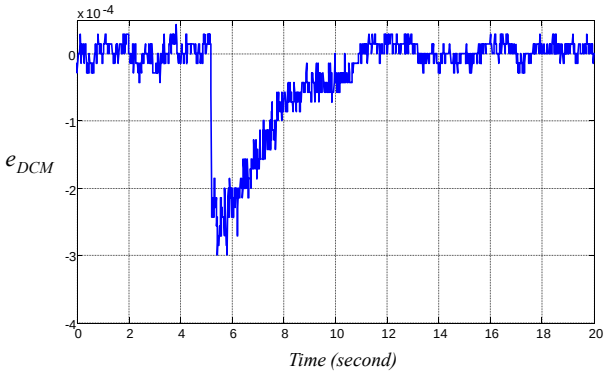

Fig. 19. Experimental results. $e_{DCM} = 0$ time evolution under a 970 to 640 W load step down.

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