

# Thin film transistors based on zinc nitride as a channel layer for optoelectronic devices

C. García Núñez, J. L. Pau, E. Ruíz, and J. Piqueras

Laboratorio de Microelectrónica, Dpto. de Física Aplicada, Universidad Autónoma de Madrid, c/Fco. Tomás y Valiente 7, Madrid 28049, Spain

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Zinc nitride films were used as an active layer in thin film transistors to assess its performance in optoelectronic applications. Those nitride layers were grown by radio-frequency magnetron sputtering in Ar/N<sub>2</sub> ambient using a Zn target. Bottom- and top-gate thin film transistors were fabricated by photolithography processes. Transmission measurements for these particular layers showed an absorption edge around 1.3 eV. Normally off transistor characteristics with a threshold voltage of 6 V were obtained in the bottom-gate configuration without post-growth annealing. In the saturation region, those transistors produced enhanced output characteristics under illumination with infrared/visible light.

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Thin film transistors (TFTs) are essential devices in active-matrix liquid crystal and organic light-emitting diode displays. Although hydrogenated amorphous silicon is usually the material of choice for the TFT channel, this technology presents some issues such as the low mobility or the poor levels of stability.<sup>1,2</sup> TFTs are also based on polycrystalline silicon with an important enhancement of the field effect mobility in comparison with those based in a-Si; however, the randomly distributed grain boundaries in a high area can hinder the fabrication process.<sup>3</sup> Therefore, different organic and inorganic materials are being investigated as potential substitutes of Si. One of them is zinc nitride (Zn<sub>3</sub>N<sub>2</sub>), which is potential candidate due to its high mobility (156 cm<sup>2</sup>/Vs) and conductivity as well as its low-cost processing.<sup>4</sup> Zn<sub>3</sub>N<sub>2</sub> thin films have been tested as channel layers in thin film transistors after an annealing process, which made the Zn<sub>3</sub>N<sub>2</sub> layer transparent to the visible light.<sup>5</sup>

In this work, TFTs with different geometric configurations, bottom- and top-gate, were fabricated by lithography and etching processes using Zn<sub>3</sub>N<sub>2</sub> as active channel layer. Their output characteristics were studied as-fabricated (without thermal treatment) in dark and under infrared/visible illumination. Zn<sub>3</sub>N<sub>2</sub> layers were synthesized by radio-frequency (rf) magnetron sputtering from a Zn target. Deposited on glass substrates, those layers presented excellent electrical properties with n-type characteristics, Hall mobility values around 100 cm<sup>2</sup>/Vs for an electron concentration of  $3.2 \times 10^{18} \text{ cm}^{-3}$ , and resistivities in the  $10^{-3} \text{ } \Omega \text{ cm}$  range.<sup>6</sup> Since Zn<sub>3</sub>N<sub>2</sub> tends to transform into zinc oxide (ZnO) at room temperature and atmospheric pressure,<sup>7</sup> the channel layers were capped with a ZnO thin layer which inhibits the reaction with the ambient oxygen and increases the stability of the devices overtime. Optical properties of those nitride layers were analyzed here by means of transmission spectroscopy in the photon energy range from 1 to 3 eV. The morphology of the Zn<sub>3</sub>N<sub>2</sub> sample surfaces was examined by scanning electron microscopy (SEM, Philips XL30) at 20-kV operation voltage.

Bottom-gate TFT was first fabricated using mechanical masking and photolithography processes. A cross-sectional schematic of the fabricated transistor is shown in Figure 1.

The Si(100) substrate was previously cleaned with ethanol, rinsed in deionized water, and blow-dried with N<sub>2</sub>. The surface area of the Si(100) substrate was around 5 cm<sup>2</sup>. A 140-nm thick Cr layer was deposited as the gate electrode by rf-magnetron sputtering. Half of the area was covered by a mechanical mask, while the remaining area was covered by a 200-nm thick SiO<sub>2</sub> layer at room temperature by electron cyclotron resonance (ECR) to form the dielectric layer. A 182-nm thick Zn<sub>3</sub>N<sub>2</sub> thin film was grown as the channel layer on top of the dielectric layer by rf-magnetron sputtering from a Zn (99.995% purity) target using a N<sub>2</sub> (99.999% purity) as working gas. Other growth conditions were 298-K substrate temperature, 30-sccm total gas flow, 1 Pa growth chamber residual pressure, and 200-W rf-power. The surface morphology of a Zn<sub>3</sub>N<sub>2</sub> layer deposited on a piece of Si(100) wafer at the same conditions than those used to grow the channel layer in the bottom-gate TFT is showed in Figure 2(a). The electrical properties of that layer were analyzed by Hall effect measurements using the four probe Van der Pauw technique and results showed a mobility around 5 cm<sup>2</sup>/Vs with resistivities and carrier concentrations around  $4.3 \times 10^{-3} \text{ } \Omega \text{ cm}$  and  $3.5 \times 10^{20} \text{ cm}^{-3}$ , respectively. The channel layer was covered with a 20-nm thick ZnO cap layer. That layer and its

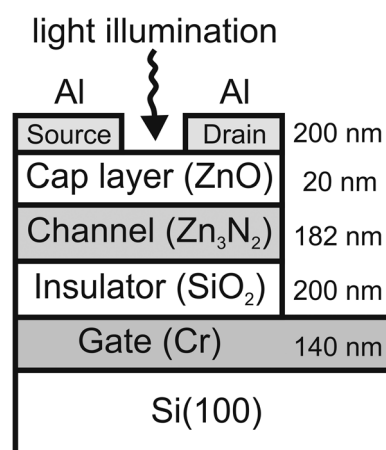


FIG. 1. Cross-section schematic of the bottom-gate Zn<sub>3</sub>N<sub>2</sub> TFT.

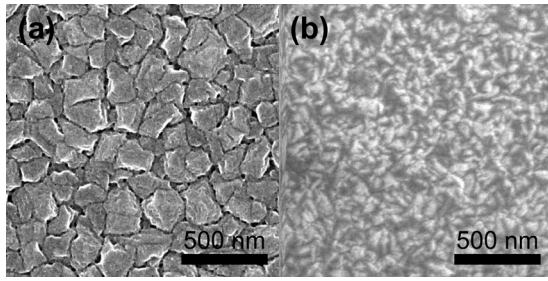


FIG. 2. SEM images of a  $\text{Zn}_3\text{N}_2$  layer used as channel in (a) bottom- and (b) top-gate configurations.

cap layer were grown one after each other to prevent surface degradation due to the ambient exposure.<sup>8</sup> Finally, a 200-nm thick Al layer was evaporated and patterned by photolithography and lift-off processes to form pairs of drain/source electrodes with different channel lengths  $L = 2\text{--}20\ \mu\text{m}$ . The width to length ( $W/L$ ) ratio ranged between 250 and 2500.

Top-gate TFTs were fully fabricated by optical lithography. The cross-sectional schematic and the top image of one of the resultant transistors are shown in Figure 3. Drain and source pair of electrodes were directly evaporated (200-nm thick film) and patterned by photolithography and etching processes on top of a oxidized Si(100) wafer substrate. Two different metals (Au and Al) were studied as metals for drain/source electrodes. Results showed that the conductance improved near an order of magnitude using Au instead of Al which can be explained as an improvement of the contact resistivity between metal and  $\text{Zn}_3\text{N}_2$ . The reason for it could be found in the oxidation of the Al contact during the electrode patterning stage. The conductive channel consisted of a  $\text{Zn}_3\text{N}_2$  layer grown by rf-magnetron sputtering. Growth parameters were 423-K growth temperature, 4.4-nm/min growth rate, and 73%-rich  $\text{N}_2$  ambient. The surface morphology of a  $\text{Zn}_3\text{N}_2$  layer deposited on a piece of Si(100) wafer at the same conditions than those used to grow the channel layer in the top-gate TFT is shown in Figure 2(b). SEM study shows less defined grain boundaries in comparison with the

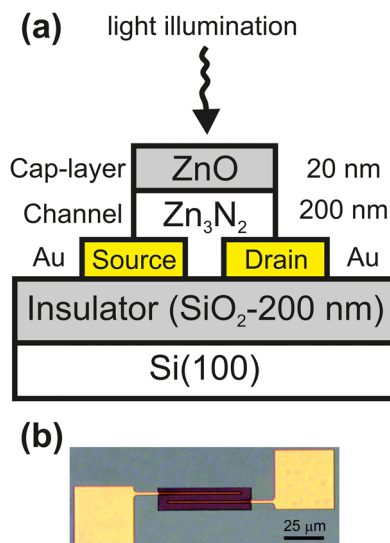


FIG. 3. Top-gate  $\text{Zn}_3\text{N}_2$  TFT (a) cross-section schematic and (b) top image taken by optical microscopy.

$\text{Zn}_3\text{N}_2$  layer used in bottom-gate TFT (Figure 2(a)) which can have a positive impact on the electrical properties of the channel layer. An insulating 20-nm thick ZnO layer atop  $\text{Zn}_3\text{N}_2$  layer was deposited by rf-magnetron sputtering in order to prevent surface oxidation. The channel layer was patterned by photolithography and chemical etching to open a window on the source and drain contacts. The channel width was  $124\ \mu\text{m}$  whereas  $W/L$  ratios equal to 7.75, 15.5, 31, and 62 were defined by varying the separation between source/drain electrodes.

Figure 4 shows the absorbance ( $A$ ) curve of a 400-nm thick  $\text{Zn}_3\text{N}_2$  layer. It is noticeable that the onset of the optical absorption is in the near-IR region extending down to the UV/VIS region. The absorption coefficient was derived from  $\alpha(\lambda) = A(\lambda)/d$  ( $d$  = layer thickness) and shows values near  $10^4\ \text{cm}^{-1}$  just above the absorption edge which are typical of direct bandgap semiconductors. The optical bandgap ( $E_g$ ) value was determined by the following Tauc and Davis-Mott models for amorphous or polycrystalline materials:

$$\alpha = A(h\nu - E_g)^n, \quad (1)$$

where  $h\nu$  is the photon energy,  $A$  is a constant, and  $n$  is 0.5 and 2 for direct<sup>9</sup> and indirect<sup>10</sup> bandgap materials, respectively. Results of both models are shown in the inset of Figure 4. A direct and indirect optical bandgap energies of 1.3 and 1.2 eV, respectively, is in good agreement with the  $E_g = 1.23\ \text{eV}$  (direct) previously reported in the literature<sup>11</sup> for  $\text{Zn}_3\text{N}_2$  layers grown under similar conditions.

Output characteristics ( $I_D/V_{DS}$ ) of the bottom-gate TFT were measured under different gate-to-source voltages ( $V_{GS}$ ) at room temperature in a four-probe system (Karl Suss Probe Station). Results for a channel length of  $2\ \mu\text{m}$  are shown in Figure 5. The TFT is in the off-state at  $V_{GS} = 0\ \text{V}$  and needs a  $V_{GS}$  voltage higher than 6 V to drive current. Therefore, the transistor operates as an n-channel enhancement-mode field effect transistor, which is preferable to depletion-mode behaviour since device design is easier and power dissipation is reduced. Positive  $V_{GS}$  above the threshold voltage ( $V_{th} = 6\ \text{V}$ ) was necessary to attract free electrons towards the gate and form the conductive channel in the  $\text{Zn}_3\text{N}_2$  layer.

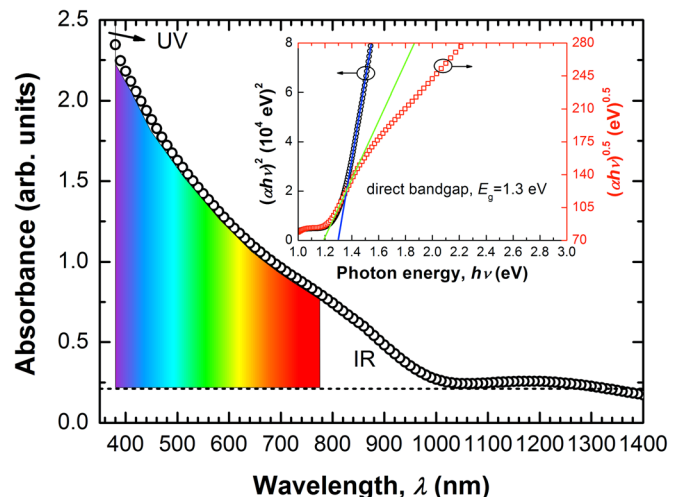


FIG. 4.  $\text{Zn}_3\text{N}_2$  transmission coefficient as a function of the photon energy. Inset: Davis-Mott and Tauc models for the bandgap type determination.

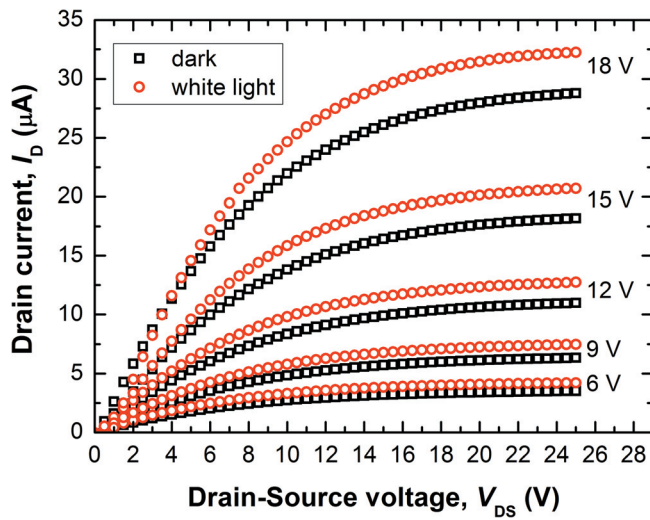


FIG. 5. Bottom gate  $I_D/V_{DS}$  characteristics in dark and under white light illumination. The channel length is  $2\ \mu\text{m}$ .

A further increase of  $V_{GS}$  above  $V_{th}$  increases the charge density in the channel so  $I_D$  increases. Saturation voltage and saturation drain current ( $I_{D,sat}$ ) also increased with  $V_{GS}$ . It is noticeable that despite the high charge concentration and the low resistivities measured in the thin films grown on glass substrates, the device is in the off-state at  $V_{GS} = 0\text{ V}$ . This behavior is believed to be caused by a charge trapping effect in the  $\text{SiO}_2$  layer since similar  $\text{Zn}_3\text{N}_2$  layer thickness provided much lower resistivity. In addition, an increase of the current is observed when the device is illuminated with a UV-filtered broadband halogen lamp. The field effect mobility ( $\mu_{FE}$ ) was estimated by using

$$I_{D,sat} = \frac{W}{L} \mu_{FE} C_{\text{SiO}_2} \frac{(V_{GS} - V_{th})^2}{2}, \quad (2)$$

where  $C_{\text{SiO}_2}$  is the capacitance of the  $\text{SiO}_2$  per unit area.  $I_{D,sat}$  was represented as a function of  $V_{GS}$  at  $V_{DS} = 25\text{ V}$  (saturation region) and using the slope of that function,  $\mu_{FE}$  was calculated to be  $0.02\text{ cm}^2/\text{Vs}$ . This value agrees well with that reported in the literature before<sup>5</sup> and was still low in comparison with those obtained in TFTs based on other materials such as a-ZnO ( $25\text{ cm}^2/\text{Vs}$ )<sup>12</sup> or GaN ( $1\text{ cm}^2/\text{Vs}$ ).<sup>13</sup> This can be associated to the high dimensions of the bottom-gate device which yield a high current leakage from the gate through the dielectric layer reducing the effective current between drain and source.

$I_D/V_{DS}$  characteristics of top-gate TFTs with different channel lengths (8 and  $16\ \mu\text{m}$ ) in dark and under a 500-nm wavelength light illumination are shown in Figure 6. The study showed linear regions at negative and positive biased voltages indicating the low resistance of both Au drain/source contacts as a result of the high carrier concentration in  $\text{Zn}_3\text{N}_2$  layers which enhanced the formation of good ohmic contacts and reduced the current crowding effect.  $I_D$  increases as the channel length decreases. In addition,  $I_D$  was in the mA range which is three orders of magnitude higher than the bottom-gate configuration at the same  $V_{DS}$ . It was corroborated the sensitivity of  $\text{Zn}_3\text{N}_2$  to the light exposure using visible light at approximately 500-nm wavelength and

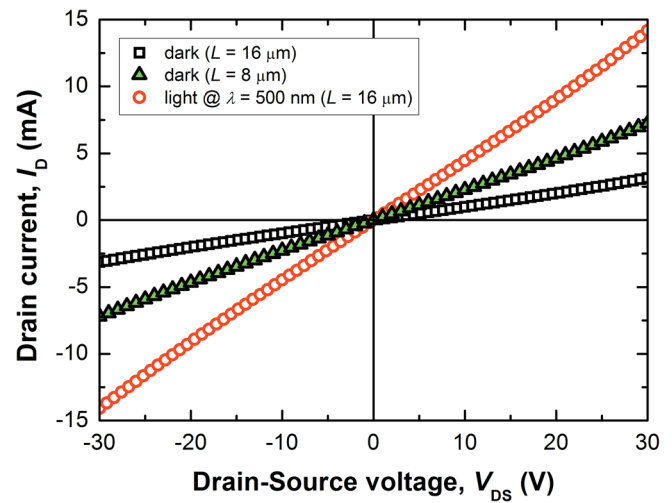


FIG. 6.  $I_D/V_{DS}$  characteristics of top-gate TFTs with 8- and  $16\text{-}\mu\text{m}$  channel length in dark and under 500 nm wavelength light illumination.

$51\text{-mW}/\text{cm}^2$  power density ( $P$ ). The photocurrent delivered is a few milliamperes above the dark current which indicates that the photoconductive gain is very high and suggests the potential application of zinc nitride in photosensing.

The photoconductivity gain ( $G$ ) was calculated in both configurations, bottom and top-gate, using expression (3)

$$G = \frac{I_{\text{photo}} h\nu}{e P A_{\text{sample}}}, \quad (3)$$

where  $I_{\text{photo}}$  is defined as  $I_{\text{light}} - I_{\text{dark}}$ ,  $e$  is the electron charge,  $P$  is the lamp power, and  $A_{\text{sample}}$  is the area of sample irradiated with a circular light beam ( $A_{\text{beam}}$ ). Gain and responsivity ( $R$ ) values for bottom- and top-gate configurations were recorded in Table I. In the table, top-gate configuration shows better  $R$  and  $G$  values than those observed in the bottom-gate configuration at 500 nm wavelength and 25 V drain-source voltage. The low dimensions and the electrical properties of the  $\text{Zn}_3\text{N}_2$  layer used in the top-gate configuration are responsible for the  $R$  and  $G$  improvement.

This work showed the use of  $\text{Zn}_3\text{N}_2$  films grown by rf-magnetron sputtering with mobilities up to  $100\text{ cm}^2/\text{Vs}$  and an optical bandgap in the energy range between 1.2 and 1.3 eV, as an active layers in bottom- and top-gate TFTs. Bottom-gate TFT output characteristics showed transistor characteristics in n-channel enhancement-mode without need of annealing process. In addition, the drain current was sensitive to the infrared/visible light illumination, showing increasing photosensitivity with  $V_{GS}$ . Top-gate TFT was fully fabricated by optical lithography and lift-off and etching processes improving  $I_D$  up to the mA range.

TABLE I. Photoconductance gain and responsivity measured at  $V_{DS} = 25\text{ V}$  and  $\lambda = 500\text{ nm}$  in top- and bottom-gate transistors  $L = 16\ \mu\text{m}$ .

	Top-gate	Bottom-gate
Electrical state	On-state	Off-state ( $V_{th} = 6\text{ V}$ )
Photogain, $G$	21828	4 ( $V_{GS} = 18\text{ V}$ )
Responsivity, $R$ ( $\text{A W}^{-1}$ )	8796	2 ( $V_{GS} = 18\text{ V}$ )

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