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Comparison of AC Mains Synchronization Methods when Using Precalculated Duty Cycles in Power Factor Correction

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Abstract— Classic PFC (Power Factor Correction) converters usually have three sensors: input voltage, input current and output voltage. Instead of using these three measures to calculate the duty cycle, precalculated duty cycles can be stored in a memory. With this memory, the system only has to synchronize with the ac mains and apply the duty cycles, at least for nominal conditions. This paper shows several methods to accomplish this synchronization, using an ADC or a voltage comparator. Results show that PFC can be achieved using simple synchronization methods and precalculated duty cycles.

Keywords—Power Factor Correction (PFC); Field Programmable Gate Array; Sensor-less control

I. INTRODUCTION

Classic PFC converters sense three signals: the input voltage, the output voltage and the input current. The sensing stage increases the cost and complexity of the system. This is magnified in the case of the current sensing, because a trade-off between power losses, cost, accuracy and bandwidth should be reached [1,2].

Digital control can be used to reduce the number of sensors of the system. For example, in [3-5] the input current measure is avoided by estimating the current using the values of the input and the output voltages.

Another approach is to avoid the current sensor using offline precalculated duty cycles which will be applied to the regulator. In this way, the system will apply those duty cycles periodically every ac mains cycle. These duty cycles can be calculated offline in a computer or with any complex system and can include electrical losses [6,7]. Using this approach, the system only needs to have synchronization with the ac mains, and no sensing is required in nominal conditions. Out of nominal conditions, the power factor quickly decreases.

Also in [8], [9] a precalculated method and its online control are presented. This control selects which set of duty cycles is output from eight possible sets by measuring only the output voltage.

Finally, in [10] several loops are added to control the output voltage and the current distortion produced by non-nominal

load when a precalculated technique is used. In that work, all the regulations are accomplished by measuring only the output voltage.

This paper is focused on the synchronization stage needed when precalculated duty cycles are to be applied to the converter switch. As there is no regulator which modulates the duty cycle, the synchronization is critical because every duty cycle must be applied in the right instant. As it will be seen, different approaches using ADCs and voltage comparators are described. Besides, switching converters are affected by electrical noise so different filters are applied and compared in the experimental results section.

II. DEVELOPMENT

In a classic topology of a PFC (Power Factor Corrector) there are two loops — i.e. the outer loop which measures the output voltage, and the inner loop which measures the input current and input voltage. In this traditional case, the ac mains synchronization is inherently done by the inner loop because it is continuously measuring the input voltage. However, systems that do not measure the input voltage to achieve PFC (Power Factor Correction) need explicit synchronization.

In this paper, several methods for ac mains synchronization are compared, using an ADC or a voltage comparator. The proposed synchronization techniques are tested in a PFC boost converter in which precalculated duty cycles are applied. As it was explained in the introduction, the precalculation technique reduces the cost of the system but the input voltage may not be measured, so the problem of synchronization arises.

The proposed system only needs to know when a new utility period starts, and then all the precalculated duty cycles can be applied (see Fig. 1). This is why ADCs or just voltage comparators can be used to achieve synchronization. The most important disadvantage of the ADC is the higher cost, as the precalculation approach is designed to reduce the cost of the converter avoiding some ADCs. ADCs have other disadvantages such as typically lower bandwidth and the non-trivial control which includes protocol interfaces, specific timing, etc. However, an ADC would be a good choice if the

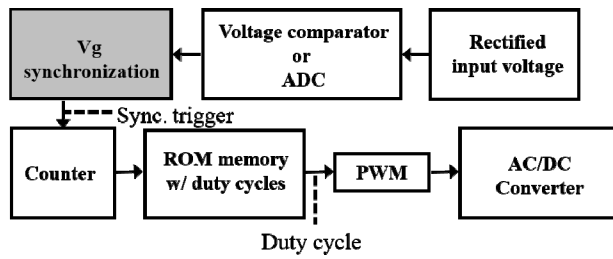


Fig. 1. Architecture of the proposed precalculated system.

system already used an ADC or if the voltage threshold to detect a new cycle is intended to be changed without hardware modifications.

All the proposed methods use comparisons between the rectified input voltage and a threshold. All methods can be applied using an ADC or a voltage comparator. Therefore, any of the following techniques can be implemented to achieve the ac mains synchronization (Fig. 1).

Method 1. Simple zero crossing detection

In the first approach the synchronization signal is triggered the first time the input voltage is smaller than a threshold so the input voltage is near zero (see Fig. 2). The choice of the threshold value is not trivial because it must be very small in order to reduce the offset between the synchronization signal and the real zero-crossing instant but it cannot be 0 V, because the input voltage probably will not reach 0 V. Moreover, this technique is very noise sensitive. If a single value is under the threshold due to noise in the measure, then the synchronization signal will generate a false trigger. This is why a more complex detector should be implemented.

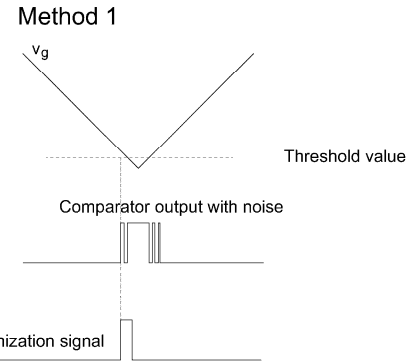


Fig. 2. Method 1.

Method 2. First and last crossing of a threshold

The comparator output (i.e. the output of the voltage comparator or the comparison with the threshold done after the ADC reading) can be digitally filtered to improve the synchronization. It will be supposed that the output is active while the input voltage is under the threshold, and inactive otherwise. Therefore, the zero crossing should be just in the middle time of active output (see Fig. 3). However, multiple threshold crossings are possible due to noise. The system uses a digital counter to measure this time but it takes into account only the first and last threshold crossing to avoid the noise. The counter value is divided by two so the result value represents the state of the counter when the input voltage crossed 0 V. This value is stored and used for the next zero crossing detection. This can be done because the counter resets again in the next threshold descending crossing and when the counter is equal to the previous stored value, the synchronization signal is triggered.

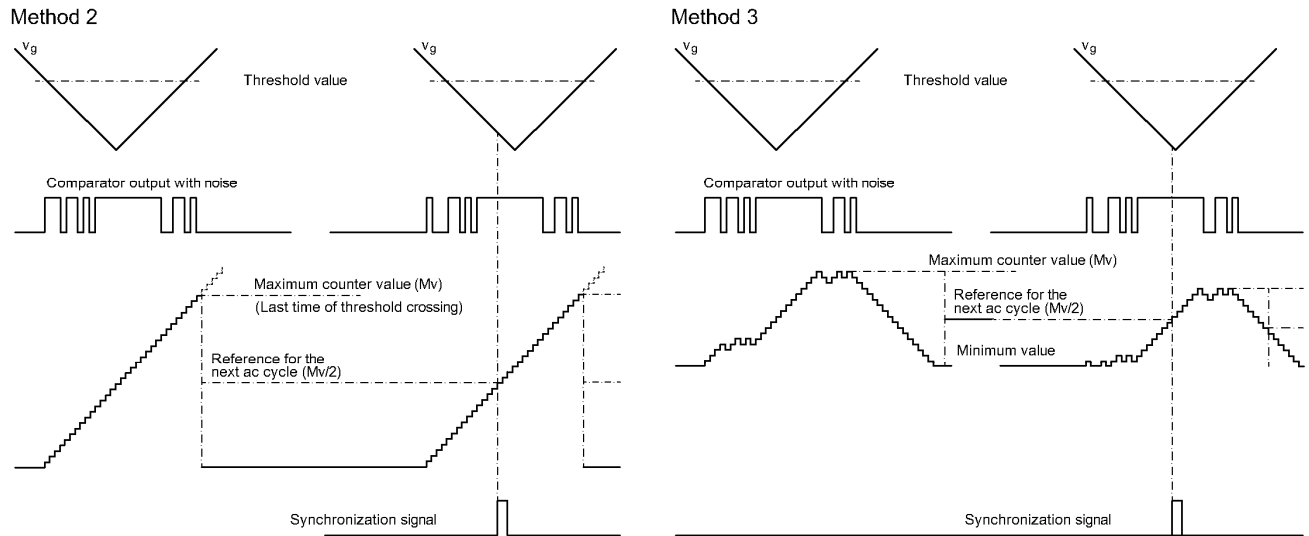


Fig. 3. Methods 2 and 3.

TABLE I. RESULTS IN NOMINAL CONDITIONS.

	M1 with ADC	M2 with Comparator	M2 with ADC	M3 with comparator	M3 with ADC
PF	0.886	0.987	0.985	0.990	0.986
Current THD	31.1%	15.2%	17.1%	15.3%	14.6%
High repeatability	No	Yes	No	Yes	No

In this case the threshold value should be a higher value (e.g. 20 V for an input voltage of 110 Vac) so the system filters electrical noises. The system acts like a filter because it gets both the falling and rising threshold crossing and these crossings are sufficiently separated in terms of time. This technique does not produce an offset in the synchronization signal, because it gets the first and last crossing of the threshold voltage.

This method is still very sensitive to electrical noise, because any fictitious threshold crossing before the real first crossing or after the real last crossing leads to wrong synchronization.

Method 3. Up/down counter depending on a threshold

The previous method does not generate an offset in the synchronization. However, erroneous synchronization is generated when there are threshold crossings produced by noise. A new filter is proposed to reduce the sensibility to noise, based also in a digital counter. Every time the input voltage is sampled, it is compared with the threshold and when it is under the threshold (e.g. again 20 V) the counter is increased by 1, and it is decreased by 1 otherwise (see Fig. 3). In this way, if noise produces a similar number of fictitious values above and under the threshold, the counter keeps unaffected. Apart from the noise, the counter is increasing when the input voltage keeps under the threshold (which it means it is near to 0 V) and is decreasing when the input voltage keeps above the threshold (far away from 0 V). This filter detects the maximum value of the digital counter and this value is divided by two and used for the next ac cycle, in a similar way than in method 2. This technique is less sensitive to noise because it does not detect the first or last time of the crossing but it calculates a pseudo-average value of the time in which the input voltage is under the threshold value. Therefore, it is expected that this method achieves better filtering results.

III. EXPERIMENTAL RESULTS

All the methods proposed in the previous section have been experimentally tested using a boost converter with the following parameters: 110 V input voltage, 200 V output voltage, output power 75 W, inductance 5 mH, output capacitance 68 μ F and switching frequency 100 kHz. The precalculated duty cycles inside an utility period are stored and they are started to be applied every time the synchronization signal is triggered. The system has been implemented using a low-cost FPGA, Xilinx XC3S1000.

Table I shows the results (PF and current THD) for all the methods explained in the previous section. There are three methods with two variations: using an ADC or a voltage

comparator. The first method has only been applied using the ADC, and the rest of the methods have been tested using both variations, so there are 5 different results.

As it can be seen, method 1 is not suitable for PFC. The main problem with the first method is the offset of the trigger. Both method 2 (using comparator) and 3 achieve good PF results for a precalculated PFC system. Methods which use comparators instead of ADCs get higher repeatability. This is because the comparator has higher bandwidth than an ADC and the quantum of error (measured in time by the FPGA) is lower than the quantum of error of the ADC — i.e. 1 LSB.

Fig 4. shows the input current using method 3 with a comparator, which is the system with the best PF results. Finally, regarding the stability of the system, the methods should detect all the ac mains zero crossing with small error to achieve high PF and avoid any damage to the power converter or the load. As it can be seen in Table I, only the second and the third method using the voltage comparator are enough repetitive to be trustworthy.

Fig 5 shows the jitter during 100 synchronization triggers for all the systems. The signals in Fig 5. have been toggled every time the synchronization signal triggers. Ideally, the jitter should be 0, and all the toggles should be overlapped. As it can be seen, method 3 with a voltage comparator is again the best method with a jitter below 16 μ s. Method 2 with ADC has more jitter than method 1 with ADC. This is because method 2 has two sources of error when there is noise: the falling and the rising edge of the rectified input voltage, while method 1 only measures the falling edge. Method 3 also measures both edges, but its filtering reduces the error produced by electrical noise.

Taking all into account, the only method which provides

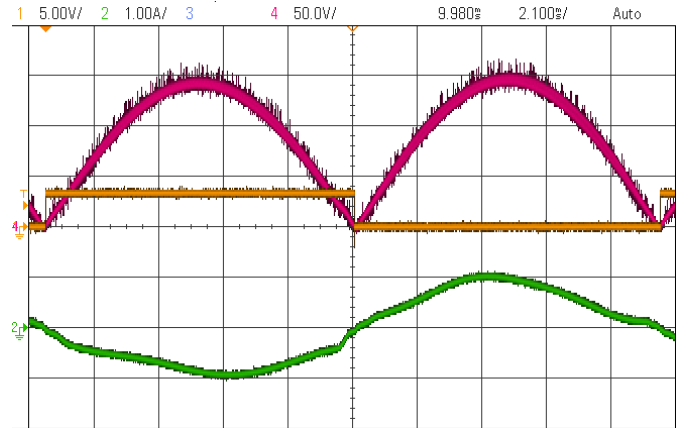


Fig. 4. Input voltage (purple), input current (green) and synchronization triggers (orange) using method 3 with a voltage comparator.

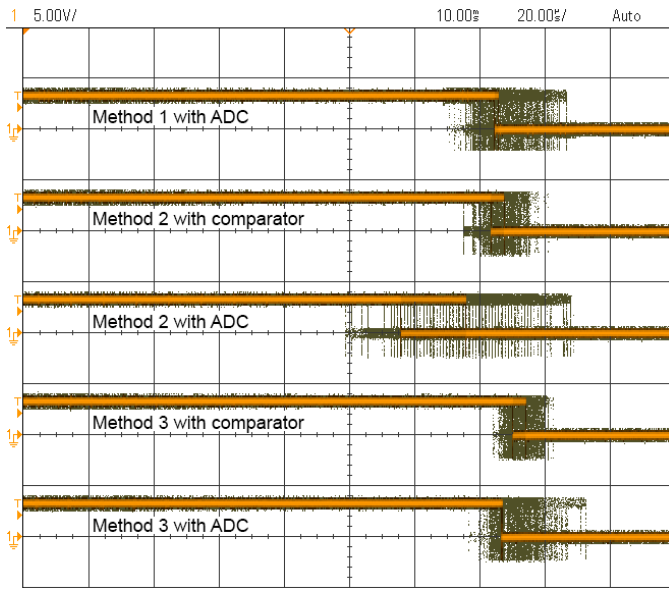


Fig. 5. Stability of the proposed systems

appropriate synchronization is method 3 using a comparator because it filters the electrical noise in the measure so high PF is reached and the system is repetitive even in the presence of electrical noise.

IV. CONCLUSIONS

Precalculated duty cycles can be applied periodically to a switching converter to get PFC. In this way, the system can reduce its cost by reducing ADCs and logic. On the other hand, precalculated PFC systems must be synchronized with the ac mains. This paper has presented three ac mains synchronization methods using an ADC or an analog voltage comparator. The first method detects the zero crossing without any filter, only comparing the input voltage with a threshold. The second method includes some filtering and improves the offset between the generated synchronization signal and the real zero crossing. Finally, the third method improves the system when

there is electrical noise in the input voltage measure. Results shows that good synchronization can be achieved using the third method and using a low cost comparator, avoiding the need of an ADC.

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