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Comparison of phase-shifters for multiphase power converters

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Multiphase power converters need multiple driving signals that must be interleaved, i.e. phase-shifted. Two alternative digital phase-shifters are proposed and compared. Both have been designed using a hardware description language, suitable for implementation in field programmable gate arrays or application specific integrated circuits.

Introduction: Much interest has been shown in multiphase switching power converters (see Fig. 1). This is due to their advantages when compared to single-phase switching power converters, such as higher current capability, improved dynamic response and reduced harmonics. They also have drawbacks, which are increased number of components, higher number of control loops (in most cases one current loop per phase) and more complex controllers that must generate multiple driving signals for the switches. Digital controllers can contribute to diminish the drawbacks of multiphase power converters [1]. For this application, those controllers implemented using custom hardware, such as field programmable gate arrays (FPGA) or application specific integrated circuits (ASIC), are especially suitable. Their concurrency (all their logic is executed in parallel and simultaneously) is very useful for generating several driving signals. This Letter proposes and compares two digital phase-shifters for the generation of multiple driving

signals. These signals must be phase-shifted between them, as shown in Fig. 2; this is known as interleaving technique. Pulse width modulation (PWM) is solved using a counter-based technique. The possible application of delay-based or hybrid techniques [2, 3] for PWM is addressed in the section dealing with comparisons.

Addition and comparison phase-shifter. The first proposed phase-shifter is based on adding some constants to the main counter and then comparing each sum to the duty cycle, as shown in Fig. 3. These sums, which are cyclic (in case of overflow, they start again from zero) are in fact equivalent to phase-shifted counters. In order to obtain homogeneous distribution along the switching cycle, the constants to be added are:

$$C_i = (i-1) \cdot \text{resol} / N \quad (1)$$

where i is the phase number from 1 to N , N the number of phases and resol the resolution of the duty cycle (number of solutions), which is equal to the range of the counter, i.e. the clock frequency divided by the switching frequency.

Shift-register phase-shifter. The second possibility is to use the driving signal of the first phase as the input of a shift-register, as shown in Fig. 4. In this way, a delay is obtained which is equal to the length of the shift-register multiplied by the clock cycle. The total length of the shift-register is at most equal to resol , while each driving signal is extracted from the position obtained by expression (1). The resulting delays are equivalent to the desired phase-shift operation.

Results and comparison: Both phase-shifters have been described in a hardware description language, VHDL, and synthesized in FPGA and ASIC devices. Fig. 2 shows the output waveforms of the FPGA implementation for 8 phases and 128 duty cycle resolution using the addition and comparison phase-shifter. The experimental waveforms with the shift-register technique are almost identical, so other comparison criteria are necessary.

The first comparison criterion is closed-loop dynamics. A duty cycle change immediately affects all the phases using the addition and comparison phase-shifter. However, using the shift-register phase-shifter only the first phase is immediately affected. Each phase delay is different, but the average delay is about half a switching period when the number of phases is high enough. In conclusion, the shift-register phase-shifter causes an additional delay of up to half a switching period, which must be taken into account for closed-loop dynamics.

The second comparison criterion is PWM resolution. The shift-register method leads to shorter critical paths (about 15% shorter) because its structure has less combinational logic. Therefore, the shift-register phase-shifter allows a somewhat higher resolution (higher clock frequency). For instance, for an 8-phase phase-shifter, the synthesis results for a Spartan-3 FPGA from Xilinx give a maximum clock frequency of 133.14 MHz when using the addition and comparison phase-shifter and 152.72 MHz with the shift-register phase-shifter. This means an increase of 14.7% in the resolution.

The third comparison criterion is how suitable is each phase-shifter for delay-based or hybrid PWM. The addition and comparison phase-shifter can be adapted including a delay-line in each phase, which demands a larger area. In the case of the shift-register phase-shifter, the shift-register should be substituted by a single delay-line, already present in a single phase delay-line PWM. So the only additional resource would be a multiplexer for each phase. Therefore, adapting the shift-register architecture is more appropriate for delay-line techniques.

The fourth and last comparison criterion is silicon area, i.e. necessary logic resources. The addition and comparison phase-shifter is very sensitive to the number of phases because each phase needs its own adder and comparator. The shift-register phase-shifter is not sensitive to the number of phases, as including more phases requires just extracting more driving signals from the already available shift-register. However, it is sensitive to the duty cycle resolution, as the length of the shift-register is proportional to it. Therefore, the shift-register phase-shifter will lead to smaller hardware structures for high number of phases and low duty cycle resolutions. To obtain the boundary between both methods, a complete set of possible configurations (changing the number of phases and the duty cycle resolution) has been synthesized. The results of the synthesis have been obtained using a complete structure that generates two complementary outputs for both the upper and lower switches, as shown in Fig. 1. A dead-time of two clock cycles between both signals is also implemented. On the left of Fig. 5 are shown the area results in

terms of occupied slices when synthesizing in an FPGA (Xilinx Spartan-3 XC3S200) with maximum effort for area optimization (synthesis tool ISE XST v10.1). Each slice contains two 4-inputs lookup tables (LUT) and two registers. The same set of configurations has been synthesized using an ASIC technology (cub_5.0V from Austria Microsystems) also with maximum optimization for area (synthesis tool Synopsys). The results in terms of total area are shown on the right of Fig. 5. It is important to take into account that each 4-inputs LUT in the target FPGA can be used as a 16-bits shift-register. This is why the shift-register technique shows better results in the FPGA than in the ASIC, and also why the number of slices increases for a low number of phases in FPGAs. It depends on whether or not the synthesis tool decides to use LUTs for the shift-register chain instead of individual registers.

Conclusions: Multiphase power converters have important advantages, but they also need a more complex controller that generates several driving signals that have to be phase-shifted (interleaved). Two alternative digital phase-shifters have been proposed. One alternative is based on additions and comparisons, while the second is based on shift-registers. Both have been described in VHDL and compared taking into account different criteria.

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Figure captions:

Fig. 1 Multiphase buck converter for dc-dc conversion

Fig. 2 Phase-shifted driving signals with FPGA implementation

Fig. 3 Addition and comparison phase-shifter hardware structure

Fig. 4 Shift-register phase-shifter hardware structure

Fig. 5 Synthesis results for FPGAs and ASICs

Figure 1

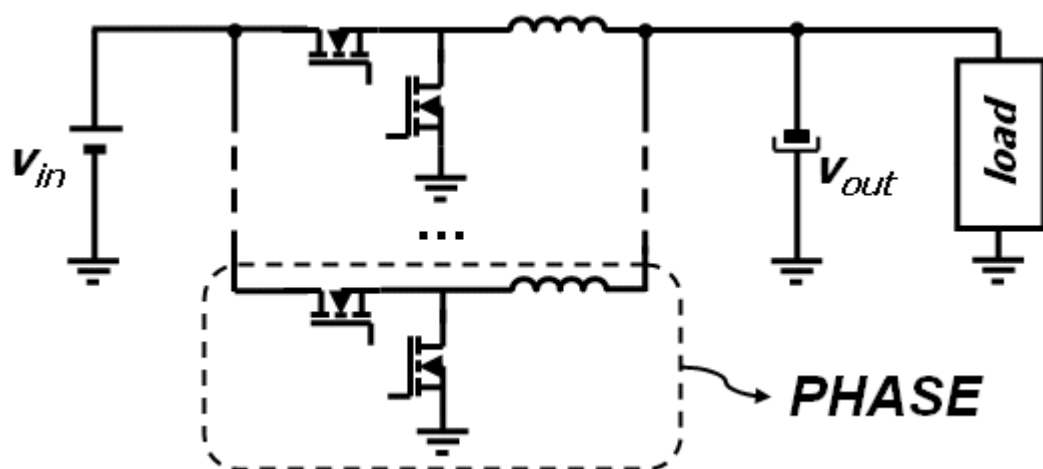


Figure 2

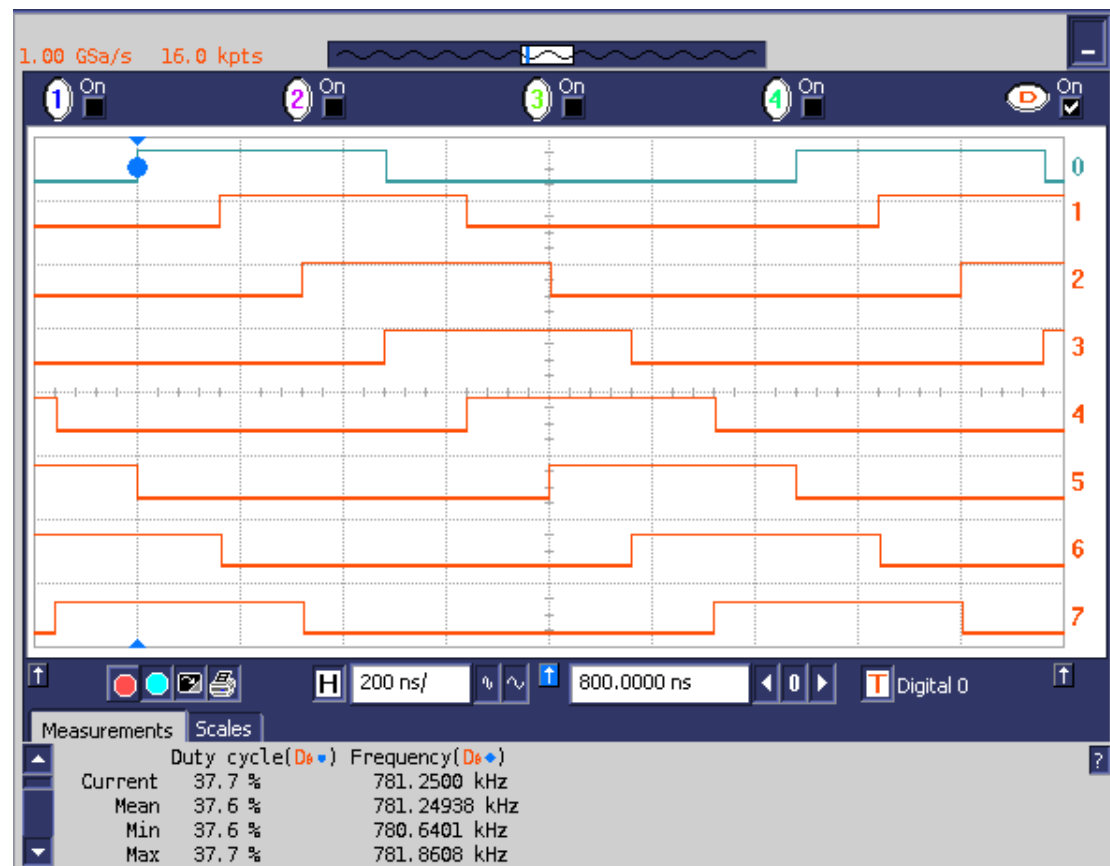


Figure 3

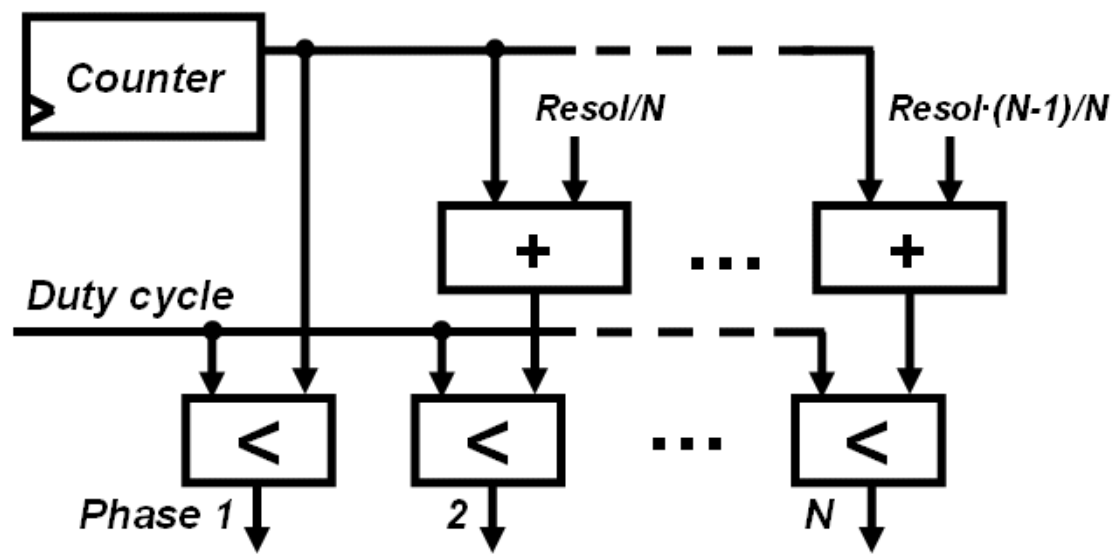


Figure 4

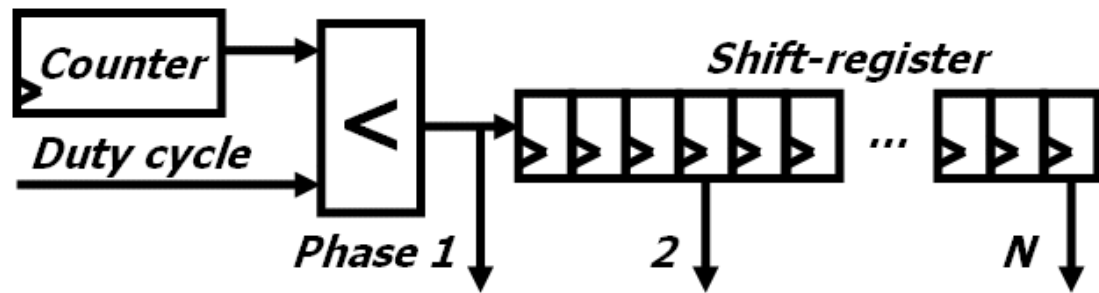


Figure 5

