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Title: Power Factor Correction without Current Sensor based on Digital Current Rebuilding

Authors: Francisco Javier Azcondo¹, Angel de Castro², Victor M. Lopez¹, Oscar Garcia³

¹Universidad de Cantabria. ETSIIyT. Av. de los Castros s/n, Santander, Spain.

²Universidad Autonoma de Madrid. EPS. Francisco Tomas y Valiente 11, Madrid, Spain.

³Universidad Politecnica de Madrid CEI. Jose Gutierrez Abascal 2, Madrid, Spain.

Corresponding author: Title: Dr. Name: Francisco Javier Azcondo

Postal Address: ETS de Ingenieros Industriales y de Telecomunicación. Universidad de Cantabria. Av. de los Castros s/n. 39005 Santander. Spain

Phone: +34942201546. Fax: +34942201873. e-mail: azcondo@ieee.org

This manuscript is an updated version of the paper presented at the IEEE Applied Power Electronics Conference and Exhibition. APEC 2009, Washington DC. USA Feb. 2009, with the title “Current Sensorless Power Factor Correction based on Digital Current Rebuilding”.

Abstract.- A new digital control technique for power factor correction is presented. The main novelty of the method is that there is no current sensor. Instead, the input current is digitally rebuilt, using the estimated input current in the current loop. The circuit measures the input and output voltage by means of low cost ad-hoc Analog-to-Digital Converters (ADCs). Taking advantage of the slow dynamic behavior of these voltages, almost completely digital ADCs have been designed, leaving only a comparator and an RC filter in the analog part. Avoiding measuring current can provide a significant advantage compared to analog controllers and this also helps reduce the total cost. The ultimate objective is to obtain a low cost digital controller that can be easily integrated as an IP block into a field-programmable gate array, FPGA, or an application-specific integrated circuit, ASIC. The experimental results show a reasonably high power factor, despite not measuring the input current, and therefore the feasibility of the method.

Key words

Power factor correction, Current mode control, Digital control, Sensorless, One-cycle control, input current estimation.

I. INTRODUCTION

There is no doubt about the interest in using digital control for switched mode power supplies (SMPS). Some of the advantages are valid for any application, for example programmability, with decreased number of components, less sensitivity to changes or noise, reduced design time and, more recently, additional power management capabilities, such as Power Management Bus, PMBus [1-2] compatibility or electromagnetic interference, EMI, reduction [3]. Some applications also obtain specific advantages using digital control, such as non-linear control algorithms that seek time-optimal performance in voltage regulator modules (VRMs) [4-6] or interleaving and current sharing in multiphase converters [7-11]. In power factor correction, PFC, most efforts of previous digital proposals have been made attempting to increase the bandwidth of the voltage loop without interfering with the intrinsic output voltage ripple [12-16]. Although the results are quite promising, the higher output voltage bandwidth can hardly compensate for the increase in price compared to the low cost analog integrated controllers and the performance is limited because the output voltage ripple will still be present even with high bandwidth voltage loops.

In some previous work, digital control was used to avoid some measurement in PFC. For instance, in [17-18] the input voltage is not measured, while in [19-21] the current is not measured and no current loop is used. In [22-23] current prediction is proposed to enhance the power section performance. It must be taken into account that the current sensor is commonly the most problematic and expensive of the three usual sensors (input/output voltages and input current) of a PFC. This work, which attempts to find a low cost digital solution, presents a controller valid for continuous and discontinuous conduction mode (CCM and DCM) operation that does not need a current sensor.

The work done includes the hardware description language (VHDL) modeling of the power and controller circuits, the design of ADCs for the measurements of the PFC input and output voltages, the design and implementation in an FPGA of the digital current estimator and the non-linear controller, and the design of the power converter. All of this work leads to a laboratory set-up focused on obtaining the characterization and optimization of the novel digital control technique.

The block diagram of the proposal is shown in Fig. 1. Both current and output loops are employed, substituting the current measurement by a digitally rebuilt current. Furthermore, the ADCs for the input and output voltages (v_{in} and v_o) have been designed ad-hoc, to find a low cost solution that can be easily integrated in CMOS technology. This is possible since the measured voltages have slow dynamics.

The rest of the paper is organized as follows. The input and output voltage sampling technique, with specific ADCs, is explained in section II. Section III is devoted to the current loop using the current rebuilding technique and gives details about the laboratory prototype used to obtain the experimental results included in section IV. After presenting the main conclusions, two appendixes have been introduced to extend the theoretical support to the analysis of the current distortion caused by the transistor drive signal delays and the output voltage ripple.

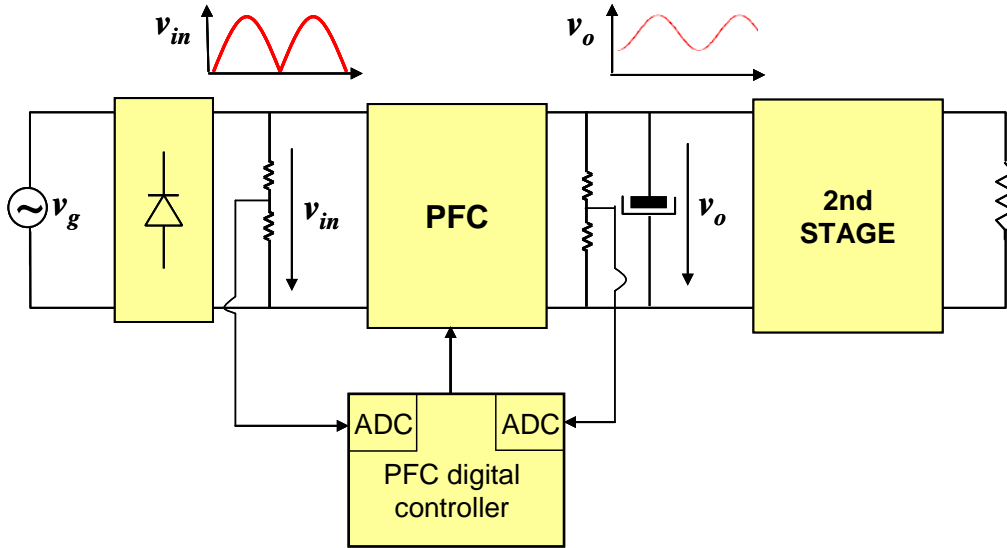


Fig. 1. PFC controller proposal

II. Ad-hoc ADCs

In the proposed controller, only the input and output voltages need to be measured. Both voltages' dynamics are defined in a low-frequency range (100 or 120 Hz for both the input and the output voltages). The proposed ADCs, which employ the $\Sigma\Delta$ principle [24], only need a comparator and a low pass filter composed of a resistor and a capacitor as analog components. The block diagram of the ADC is shown in Fig. 2.

An up/down counter represents the measured voltage as a digital bus. This bus is converted into a bitstream using a $\Sigma\Delta$ modulator (dotted line block). The bitstream is then converted to an analog voltage using an RC low-pass filter, which is compared to the analog input. Depending on this comparison, the counter is increased or decreased. The integral action of the $\Sigma\Delta$ modulator (the accumulator) guarantees that the error is zero in steady state. Therefore, the mean value of the counter (once translated into voltage) has to be equal to the measured voltage.

The main drawback of the proposed ADC is that it is quite slow: when using M bits, the clock frequency is divided by up to 2^M . However, the digital clock and the input or

output voltages have such different dynamics (up to 100 MHz and 100/120 Hz respectively in our case) that the slow nature of the ADC is not a real limitation.

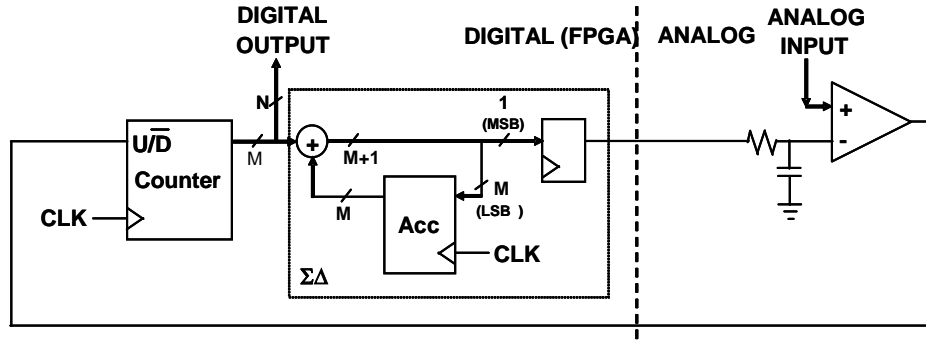


Fig. 2. Ad-hoc $\Sigma\Delta$ ADC.

The resistor – capacitor (RC) network filters the high-frequency components of the signal generated by the $\Sigma\Delta$ modulator (bitstream). The clock frequency, f_{ADCclk} , is obviously present because the modulator output is updated at this frequency. Sub-harmonics are also present, which can be as low as $f_{ADCclk}/2^M$ (M being the number of bits). Given the slow behavior of the measured voltages, in principle, the best solution would be a large RC constant, enough to filter frequencies much lower than $f_{ADCclk}/2^M$, but not reaching the measured voltage frequency. However, a large delay of the RC filter introduces oscillations in the voltage measurement. On the other hand, reducing the RC constant diminishes precision because not all the sub-harmonics are filtered. A trade-off between precision and stability has to be found. Examples of experimental results changing the RC values are shown in Table I, using a clock frequency of 50 MHz and 8 bits of resolution. Both the oscillation and the error are referred to the complete ADC resolution (i.e. error/256), giving the worst case in all the measurement ranges.

TABLE I
OSCILLATION AND ERROR USING DIFFERENT RC VALUES WITH $M = 8$

R	C	Corner frequency (kHz)	Maximum Oscillation	Maximum Error
1 k Ω	22 pF	7234	16%	7.4%
1 k Ω	220 pF	723	22%	1.5%
1 k Ω	2.2 nF	72	59%	1.1%

In order to decrease the relative oscillation, two equivalent solutions have been tested. One was selected due to its simplicity, which is to increase the number of bits. The oscillation basically remains the same independently of the number of bits, but its percentage is halved with each additional bit. The other solution is to update the counter at a slower frequency, while maintaining the same frequency in the modulator. Maximum bitstream and comparator output frequency is f_{ADCclk} . In order to preserve the signal integrity from the FPGA to the filter and from the comparator back to the FPGA, f_{ADCclk} has been reduced from 100 to 3.125 MHz. A filter $R = 2.2$ k Ω and $C = 10$ nF has been used for the experimental results shown in the rest of the paper. The ADCs have been implemented using $M = 14$ bits. However, only $N = 10$ bits has been used (the MSBs) because the oscillations affect the LSBs. In this way, 10 bits of resolution with almost no oscillation (noise) has been achieved.

III. DIGITALLY REBUILT CURRENT

The main contribution of the proposed controller is that the input current does not need to be measured. Instead, it is digitally rebuilt from the input and output voltages together with the on/off driving signal. In the case of a Boost converter, which has been used in the experimental results, the input current increases proportionally to v_{in} during the on-time, while it decreases proportionally to $v_{in}-v_o$ during the off-time (see Fig. 3). The rebuilding algorithm changes slightly in each topology, but can be easily adapted.

The on and off times are known within the controller because the driving signal is generated there, so a simple accumulator can represent the estimated current.

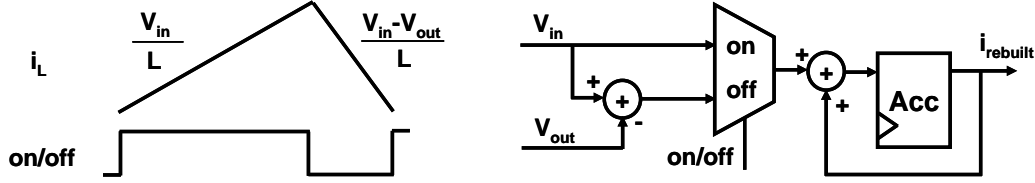


Fig. 3. Current rebuilding concept. Waveforms (left) and HW architecture (right)

It must be taken into account that the rebuilding update frequency, which is the clock frequency, f_{clk} , in this case, sets the resolution of the pulse-width modulation (PWM). Therefore, the rebuilding technique is more appropriate for custom hardware (FPGA or ASIC) implementation than for digital signal processor (DSP) or microcontroller, as in [25-26].

The input current control loop shapes the rebuilt current, $i_{rebuilt}$, while the output voltage control loop generates the current reference, i_{ref} , for the utility period as depicted in Fig. 4.

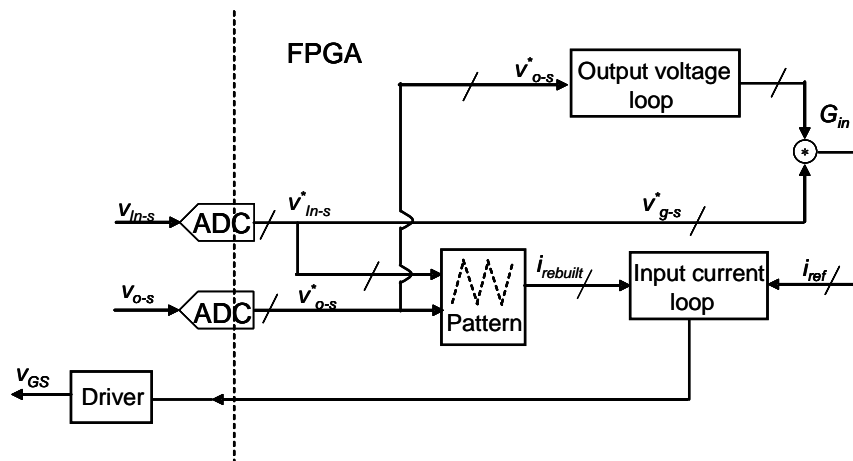


Fig. 4. Schematic of the sensor-less current controller

Although simulation of the converter model under the proposed control shows perfect current shaping, as is shown in Fig. 5, even considering inductance tolerances, the experimental results have shown that the most critical errors are due to: a) The drive

signal's delays, especially when the on-to-off delay is different from the off-to-on delay, because the effective duty cycle is changed, b) Measured voltage errors due to offsets and c) Measured voltage errors due to sample and hold and registering delays. A theoretical analysis of the effect of the drive signal's delays is presented in Appendix I. The contribution of the output voltage ripple to the current distortion is evaluated in Appendix II concluding that this contribution is lower than the uncompensated drive signal delays.

An effect of the accumulative inductance volt-seconds error is shown in Fig. 6, where the volt-seconds across the inductor in each switching period are different to the calculated values. Therefore, the input current, i_{in} , does not grow as required and calculated by $i_{rebuild}$. Later, since the low i_{in} affects the output voltage, the input current rise during the on-time is not properly compensated for in the off-time and i_{in} increases differently than desired. This effect is experimentally confirmed.

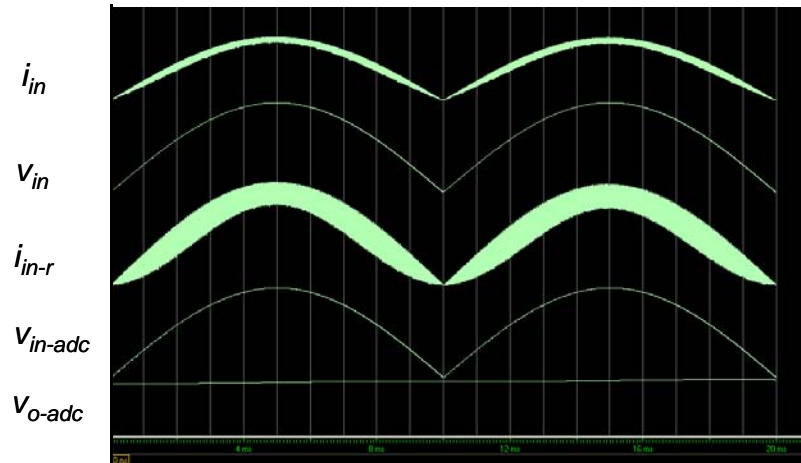


Fig. 5. Simulation of the PFC under the proposed sensor-less control. From top down: input current, input voltage, rebuilt input current, digital samples of the input voltage and digital samples of the output voltage

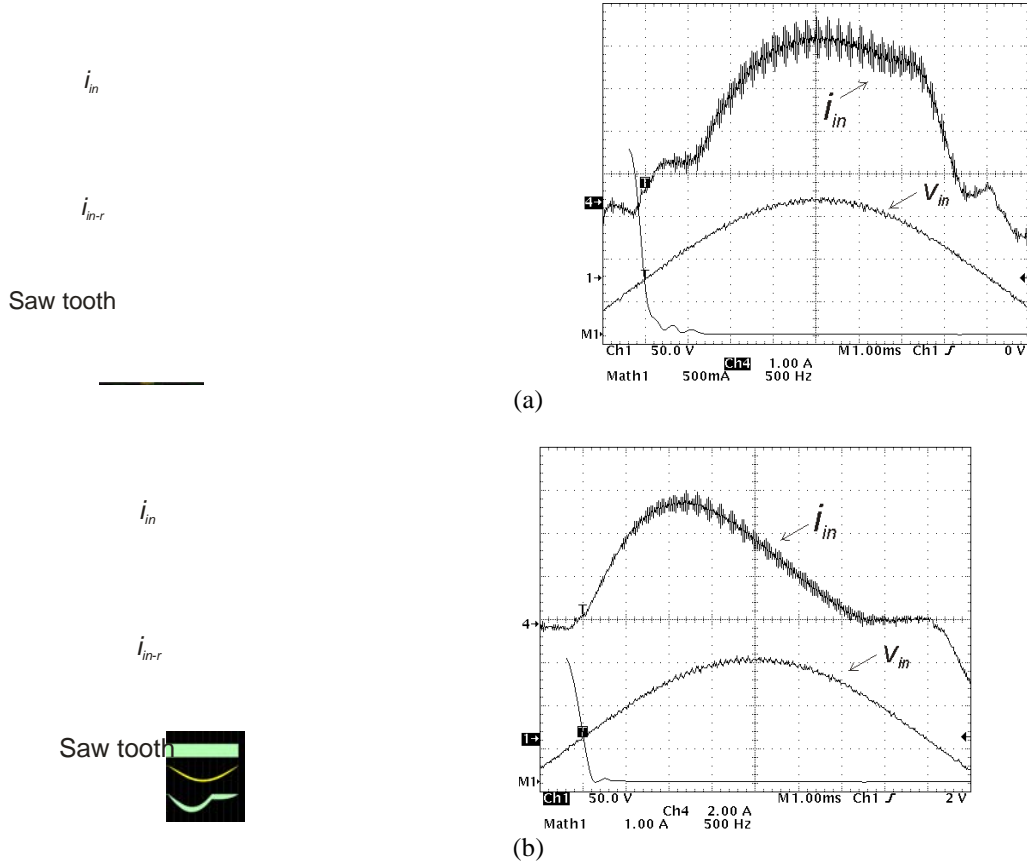


Fig. 6. Effect of the accumulative volt-seconds error. Left simulation: Top input current. Middle rebuilt current, bottom carrier control signal. Right experimental scope captures: Top input current. Middle input voltage and bottom FFT of the input current. (a) Case when the calculated volt-seconds value is lower than the actual volt-seconds applied to the inductance (b) Case when the calculated volt-seconds value is higher than the actual volt-seconds applied to the inductance.

If the delay difference is known or measured, it can be compensated for in the rebuilding algorithm. Since the accumulative error due to delays and offset is the difference between the volt-seconds applied to the inductor and the value calculated by the digital circuit, the compensating technique can be unified using a single variable.

Sample and hold and register delays, τ_{SH} and τ_R respectively, produced in the v_{in} and v_o data acquisition process, cannot be compensated for by compensation constants. As is observed in Fig. 7, where the fundamental components of the digitally rebuilt v_{in} affected by τ_{SH} and τ_R are represented, the sign of the error depends on the voltage slope. The slow rate of change of the measured voltages enables the implementation of effective compensation by the linear extrapolation of the voltage acquired data. Since

the current calculation frequency, f_{clk} , is higher than f_{ADCclk} the voltage values are calculated adding and incrementing Δv_{in} , over the previous value

$$\Delta v_{in} = \frac{(v_{in}[n] - v_{in}[n-1])f_{clk}}{f_{ADCclk}}, \quad (1)$$

where $v_{in}[n-1]$ and $v_{in}[n]$ are the last two samples

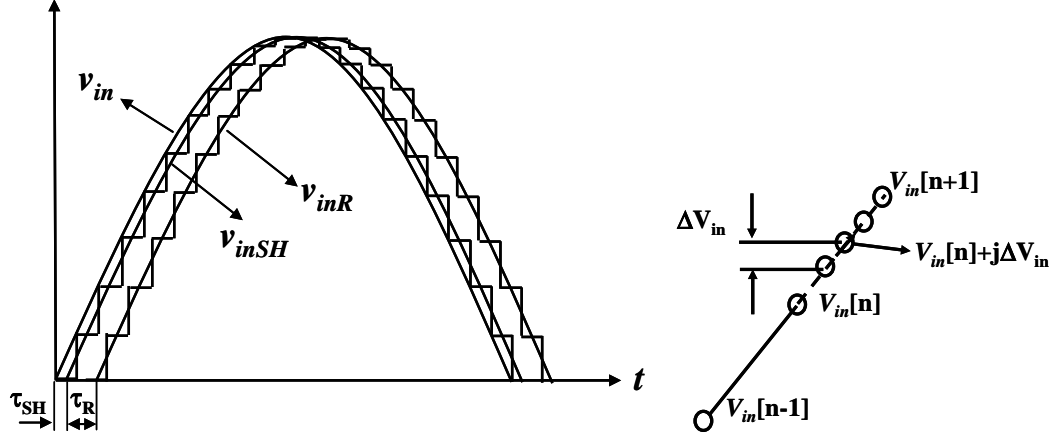


Fig. 7. Left, representation of v_{in} affected by the sample and hold, and the register delays. Right, linear extrapolation.

Once the input current is rebuilt, any current loop can be used: average current, peak-current, hysteric control, etc. In this proposal, one-cycle control is used [27-30], which has the advantage of using constant switching frequency that can be easily implemented in digital hardware, because it is based on additions and comparisons.

Nonlinear one-cycle controllers compare a carrier signal with the variable under control, in this case the rebuilt input current, to determine the switching instant. Fig. 8 shows the case for the Boost converter. The turn-off instant corresponds to

$$V_m - V_m \frac{t_{on}}{T_s} = r_s i_{Lpk}, \quad V_m(1-d) = r_s i_{Lpk}, \quad (2)$$

where r_s is the virtual current sensor resistor, i_{Lpk} is the maximum $i_L = i_{in}$ in the switching period, T_s , V_m is the maximum carrier signal value controlled by the outer loop, and d is the duty cycle. In CCM steady state, the control law is rewritten as

$$V_m \frac{v_g}{V_o} = r_s i_{Lpk}, \quad (3)$$

and, therefore, the peak current follows the input voltage in each switching period, achieving power factor correction. One-cycle control can be modified in order to be adapted to other topologies. For example, in a Buck-Boost type converter, e.g. SEPIC, the turn-off instant corresponds to

$$V_m - V_m \frac{t_{on}}{T_s} = r_s i_{Lpk} \frac{t_{on}}{T_s}, \quad V_m \frac{1-d}{d} = r_s i_{Lpk}, \quad (4)$$

to ensure that the peak current is proportional to v_{in} in each switching period.

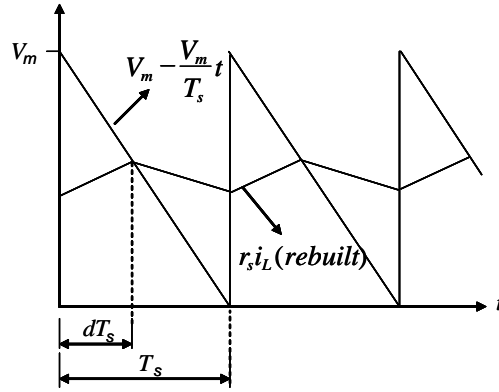


Fig. 8. One-cycle control for the Boost converter controlled as PFC

The parameter V_m is the result of the outer output voltage control loop. In steady state V_m represents the line power,

$$P_{in} \cong V_m \frac{V_{in}^2}{r_s V_o}. \quad (5)$$

Accumulative volt-seconds errors caused by v_{in} and v_{out} data deviations or by switching delays are compensated for by generating the transition of the switch drive signal before the theoretical conditions come into effect. Compensation times are introduced for the on-off and off-on switching times, defining the parameters n_{dlon_off} as the number of clock cycles equivalent to the delay in the on-off transition and n_{dloff_on} in the off-on transition. The on-off transition is generated by the digital circuit clock periods ($n_{dlon_off} \cdot T_{clk}$) before reaching condition (2) and the off-on transition is generated n_{dloff_on} clock periods before the carrier ramp reaches zero. Fig. 9 represents the

modification introduced in the one-cycle control algorithm to compensate for the inductor volt-seconds error, where the ideal drive signal is the “non-compensated” one. In order to compensate for the delays, the FPGA generates the “compensated” signals instead. Once they travel through the driver and switch, the real pulses will be almost identical to the “non-compensated” signal, which is the desired behavior.

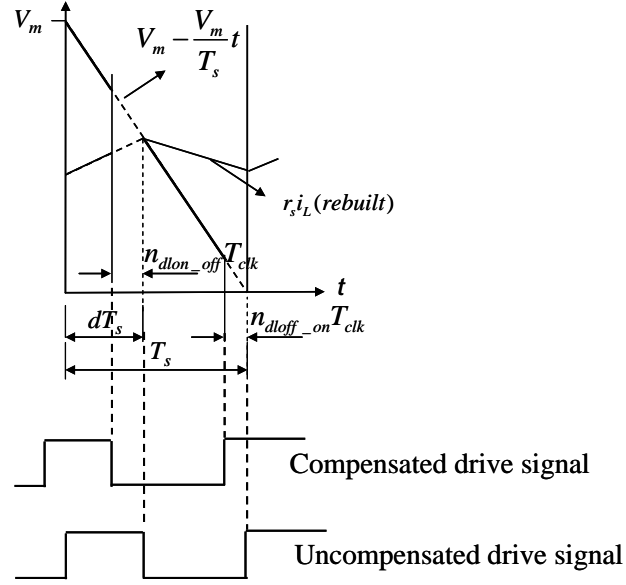


Fig. 9. Modification of the one-cycle algorithm to compensate for inductor volt-seconds errors

The converter model, stimuli and digital controller design are all described in VHDL [31-32], resulting in projects developed in a single design framework that includes digital simulation and synthesis tool.

The *Test Bench* file defines the circuit stimuli, reads the outputs of the power converter and defines the connections among the project components. The utility voltage source and the power converter load (defined either as a resistor or as a current sink, depending on a Boolean signal) are the main inputs, while the utility current and power converter output voltage are the main outputs. The *Clock* and *Reset* signals synchronize the operation of the digital circuits. Two signals, which are associated with the sample of the power converter input and output voltage, connect the power section with the input to the ADCs' comparators. Another two signals allow the connection

between the comparators' output and the digital section of the ADCs. As shown in Fig. 10, the digital circuit generates two output signals (bitstreams), also defined in the test bench description, which are filtered in the analog part of the ADCs, and the *on-off* signal that defines the state of the power switch.

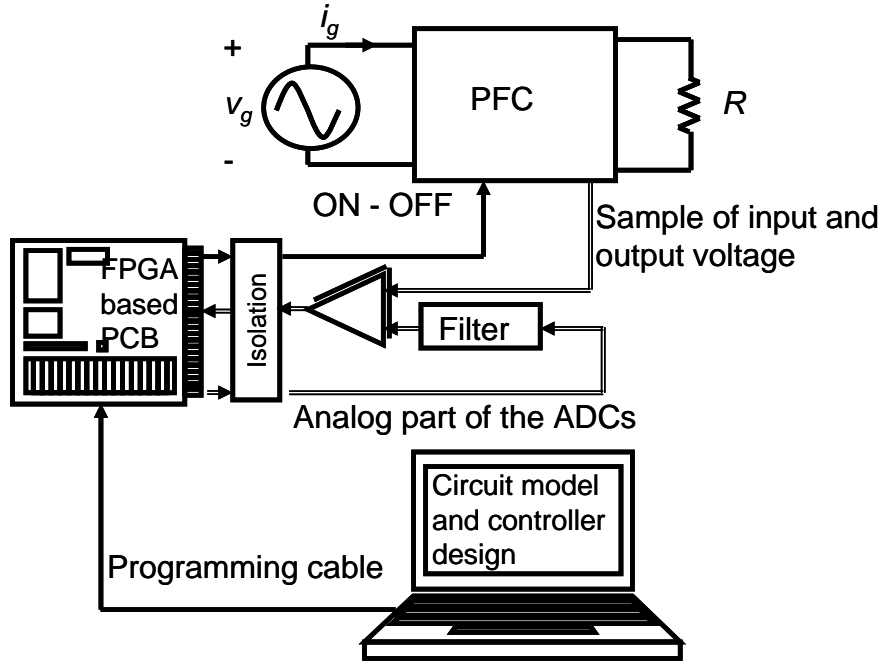


Fig. 10. Block diagram of the laboratory set-up

The *Test Bench* also includes the instantiation of: 1) the power converter model, 2) the PFC controller and 3) the digital and analog parts of the ADC. As an illustrative example, Fig. 11 shows the VHDL description of the boost converter on-state circuit.

Four processes define the circuit stimuli: 1) Digital circuit clock, 2) Initialization that defines the reset signal, 3) Description of the utility voltage and 4) Description of the power converter load. A final process has been defined to model the delay between the power switch drive signal edge and the actual power device off-on and on-off transitions.

```

Iin <= IL;
Vo <= VoAux;

CALC: process
-- State variables are updated each integration period
begin
  if OnOff = '1' then -- on-state
    IL <= IL + ( (Vg*dt2) / L );
    if Resist then -- Resistive load
      VoAux <= VoAux - ( (VoAux/R)*dt2 / C );
    else
      VoAux <= VoAux - ( (Ir*dt2) / C );
    end if;
  else -- off-state
    .
  .

```

Fig. 11. VHDL model of the Boost on-state circuit

IV. EXPERIMENTAL RESULTS

After simulation, a boost converter prototype was built in order to test the proposed controller. The controller and the digital parts of the ADCs were implemented in a Spartan-3E XC3S500E Xilinx FPGA evaluation board. The ADCs were implemented as explained in section II with $M = 14$ bits of resolution, although only the $N = 10$ MSBs have been used (the 4 LSBs exhibit noise). The boost converter used in this experiment was designed for V_{in} up to 220 V_{rms}, 50 or 60 Hz, 500 W and f_{sw} 73 kHz (it was an existing prototype, not designed for this purpose). No line filter is included for the experiments. The circuit implementation schematic is presented in Fig. 12. Bitstream signals and unipolar comparator output signals link the FPGA to the filter and comparator devices through IL712 isolators. Connection between the FPGA and the MOSFET gate is performed through a HCPL3120 driver.

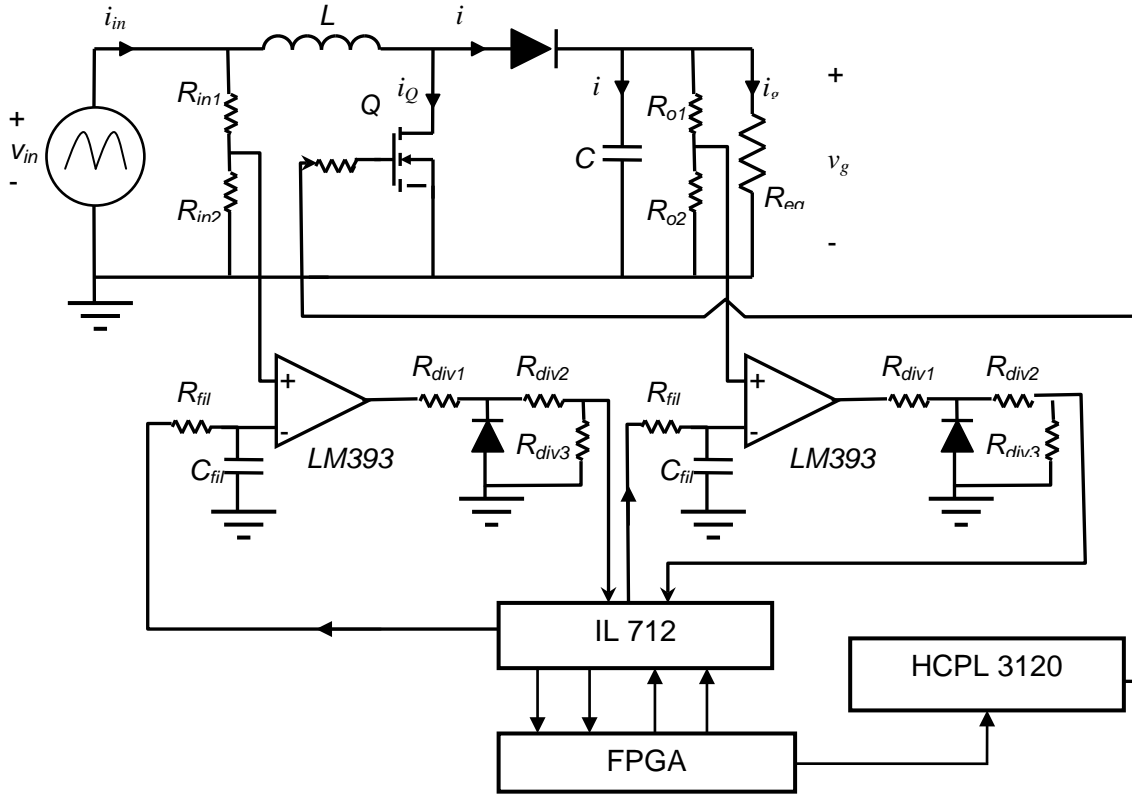


Fig. 12. Experimental PFC circuit and control schematic

Fig. 13 to 17 show different aspects of the PFC operation under the proposed control. In Fig. 13 the FPGA output (channel 1) that acts as the MOSFET drive signal is compared to the inductor voltage (channel 2). The measured delay time is 520 ns for the on-off transition and 460 ns for the off-on transition. These delays are used in the n_{dlon_off} and n_{dloff_on} parameters of the controller.

Fig. 14 presents the results of the data acquisition. The input voltage and the corresponding filtered bitstream obtained from the circuit in Fig. 2 are shown. No significant delay is observed although the noise may induce some perturbation in the input current.

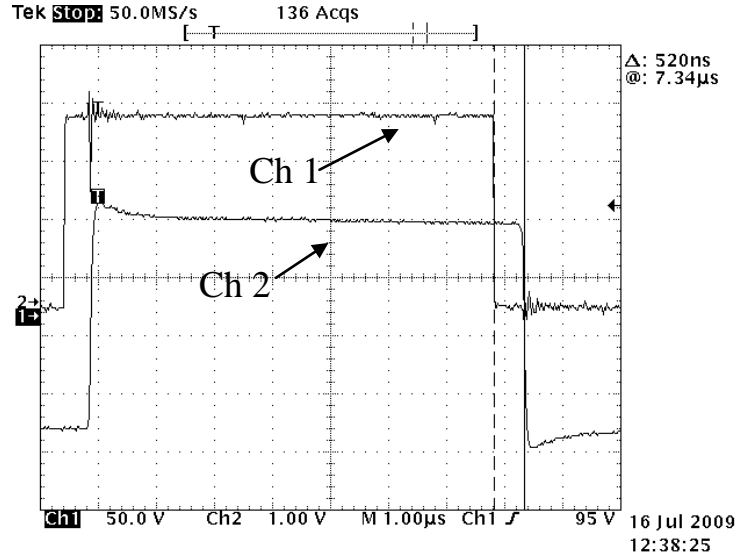


Fig. 13. Experimental time switch transitions compared with the drive signals. Ch1, MOSFET drive signal FPGA output. Ch2, Inductor voltage

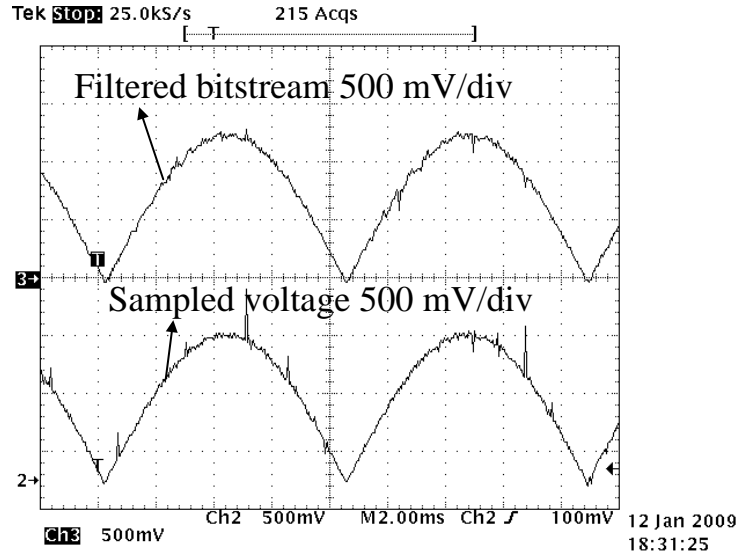


Fig. 14. Experimental data acquisition on input voltage.

Fig. 15 (a) shows v_g (channel 1) and i_g (channel 4), for the utility voltage $V_g = 120V_{rms}$, 60 Hz, and output power, $P_o = 400$ W. Fig. 15 (b) shows the same waveforms at $V_g = 230 V_{rms}$, 50 Hz, $P_o = 416$ W. It can be seen that current shape is very good for the first case ($V_g = 120$ V). The current waveform in the second case ($V_g = 230$ V) shows some more distortion and a higher frequency current ripple (it should be noted that no line filter is included in the prototype). Power factor correction was successfully achieved. Measurements of power factor were 0.99 in the first case

and 0.98 in the second. The harmonic content of this waveform complies with regulation EN61000-3-2 for class C lighting application equipment (the most restrictive). Measured delays within the utility period, for input voltage 70 to 230 V_{rms} and output power 200 to 600 W, as shown in Fig. 13, range from 520 to 700 ns in the on to off transient and from 440 to 500 ns in the off to on transient.

Values of compensation that enables the fulfillment of EN61000-3-2 class C in different cases are $n_{d\text{lon_off}} = 56$ and $n_{d\text{loff_on}} = 53$, equivalent to 560 ns and 530 ns respectively.

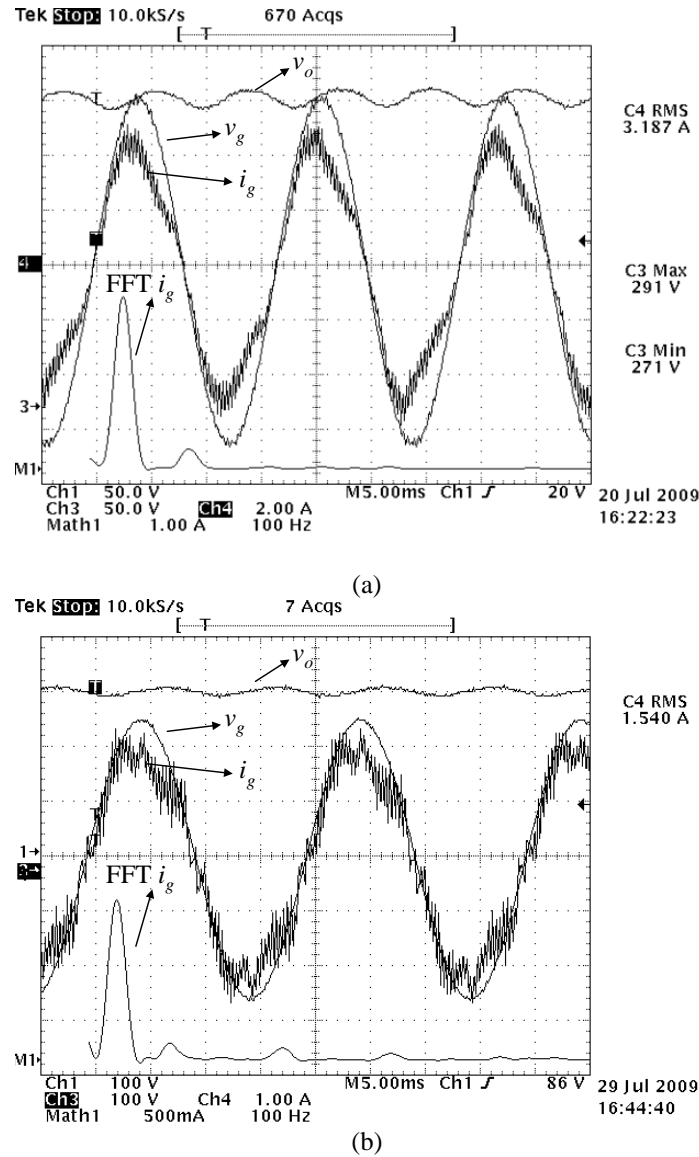
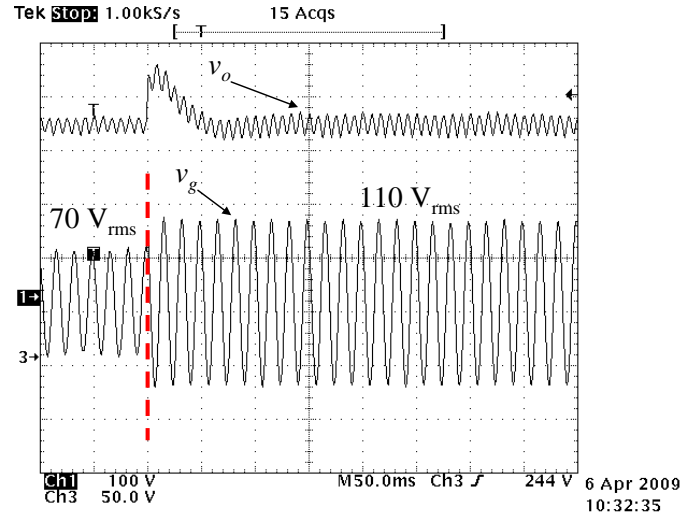
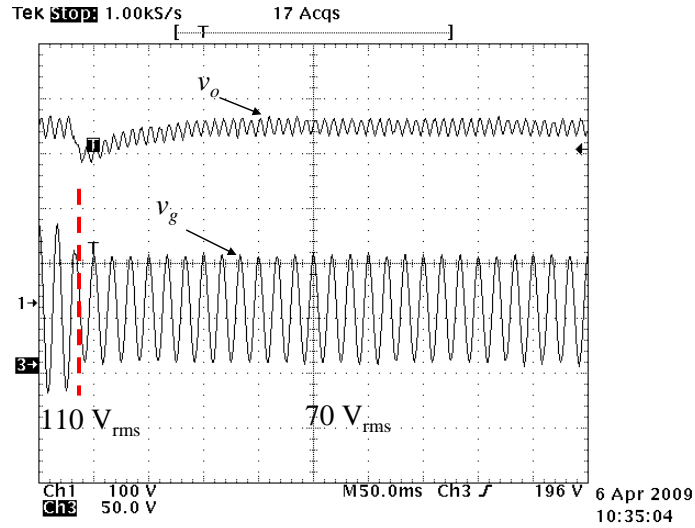


Fig. 15. Experimental results. (a): $V_g = 120 \text{ V}_{\text{rms}}$, 60Hz. Ch. 1 input voltage, ch. 3 output voltage, ch. 4 input current, math 1 input current spectrum. (b): $V_g = 230 \text{ V}_{\text{rms}}$, 50Hz. Ch. 1 input voltage, ch. 3 output voltage, ch. 4 input current, math 1 input current spectrum.

As a proof of concept, the outer loop has been designed using a basic integral action. In Fig. 16 the output voltage response under input voltage step transients from $V_g = 70V_{rms}$ to $V_g = 110 V_{rms}$ and vice versa are presented. Output voltage stabilization completes the PFC digital control action.



(a)



(b)

Fig. 16. Outer loop response under input voltage step changes. (a) positive input voltage step, (b) negative input voltage step

V. CONCLUSIONS

A digital controller for power factor correction has been proposed. Taking advantage of digital circuit capabilities, the input current is rebuilt from the input and output voltages instead of being measured. Avoiding the current measurement can be a significant advantage with respect to analog controllers, which also helps to reduce the total cost. Taking advantage of the slow nature of the input and output voltages, cheap ad-hoc $\Sigma\Delta$ ADCs have been designed. Their only analog components are a comparator, a resistor and a capacitor. The ADCs' digital blocks are integrated with the rest of the controller and the digital controllers of subsequent power stages could also be integrated in the same device. The difference in volt-seconds across the inductor between the estimated values in the ideal and the real cases causes utility current distortion. Compensation of this effect has been included in the control algorithm. A high digital circuit clock frequency is required to achieve adequate compensation resolution. The control circuit has been tested using 100 MHz clock frequency (10 ns of time compensation steps). Compensation values enabling the PFC circuit to meet the EN61000-3-2 class C limits have been proven valid for a quite broad utility voltage and load range, however, a specific compensation is not universal. PF and THD change under variations of the utility voltage and load. Further research work is being done to extend the validity of the compensation parameter and even to achieve auto-compensation. The experimental results show the feasibility of the method, obtaining a high power factor in spite of not measuring the input current.

APPENDIX I. ANALYSIS OF THE EFFECT OF THE DRIVE SIGNAL'S DELAY

Using (2) and (3) and considering no drive signal delay and output voltage with no ripple, V_o , the volt-seconds across the inductor, v_{sL} , over half the utility period, $[0, T_u]$, are given in (6) and (7) for the on and off time respectively.

$$vS_{L,on} = \sum_{n=1}^{\frac{T_u}{T_s}} \langle v_{in} \rangle_{t_{on_n}} \left(1 - \frac{\langle v_{in} \rangle_{t_{on_n}}}{V_o} \right) T_s \quad (6)$$

$$vS_{L,off} = \sum_{n=1}^{\frac{T_u}{T_s}} \left(\langle v_{in} \rangle_{t_{off_n}} - V_o \right) \frac{\langle v_{in} \rangle_{t_{off_n}}}{V_o} T_s, \quad (7)$$

where $\langle v_{in} \rangle_{ton_n}$ and $\langle v_{in} \rangle_{toff_n}$ are the input voltage of the switching period n averaged in the on and off time respectively.

If the difference between the drive signal positive and negative edge delay and the corresponding compensation are Δt_{off-on} and Δt_{on-off} respectively, (6) and (7) become (8) and (9),

$$vS_{L,on} = \sum_{n=1}^{\frac{T_u}{T_s}} \langle v_g \rangle_{(t_{on_n} + \Delta T_s)} \left(1 - \frac{\langle v_{in} \rangle_{(t_{on_n} + \Delta T_s)}}{V_o} + \Delta d \right) T_s \quad (8)$$

$$vS_{L,off} = \sum_{n=1}^{\frac{T_u}{T_s}} \left(\langle v_{in} \rangle_{(t_{on_n} + \Delta T_s)} - V_o \right) \left(\frac{\langle v_{in} \rangle_{(t_{on_n} + \Delta T_s)}}{V_o} - \Delta d \right) T_s \quad (9),$$

where $\Delta T_s = \frac{\Delta t_{on-off} + \Delta t_{off-on}}{2}$ and $\Delta d = \frac{\Delta t_{on-off} - \Delta t_{off-on}}{T_s}$ account for the switching

period displacement and the duty cycle modification respectively. For simplicity's sake Δt_{off-on} and Δt_{on-off} are assumed constant.

The addition of (8) and (9) computes the inductor current variation, which is zero at $t = T_u$, when delays are compensated for and produces distortion otherwise.

$$vS_L = vS_{L,on} + vS_{L,off} \quad (10)$$

Imposing the average inductor current over the switching period, $\langle i_{in} \rangle_{T_s} = 0$ at $t = 0$ as a boundary condition,

$$\langle i_{in} \rangle_{T_s} = \frac{vS_L}{L} \quad (11)$$

The difference between the non-compensated and compensated cases has been approximated in the continuous time domain and integrated over $[0, T_u]$ giving a current distortion, i_{ind} , described by expression (12)

$$i_{ind} = \frac{1}{\omega L} \left\{ V_o \omega t \left(\frac{\Delta t_{on-off} - \Delta t_{off-on}}{T_s} \right) + \hat{V}_{in} \cos(\omega t) - \hat{V}_{in} \cos \left[\omega \left(t + \frac{\Delta t_{on-off} + \Delta t_{off-on}}{2} \right) \right] \right\} \quad (12)$$

Fig. 17 presents expression (12) added to a compensated sinusoidal current for $\Delta t_{on-off} = 40$ ns and $\Delta t_{off-on} = 80$ ns as a function of time and its FFT in comparison with the EN-61000-3-2 class C limits. The result is a power factor $PF = 0.796$ and total harmonic distortion THDi 42.3%

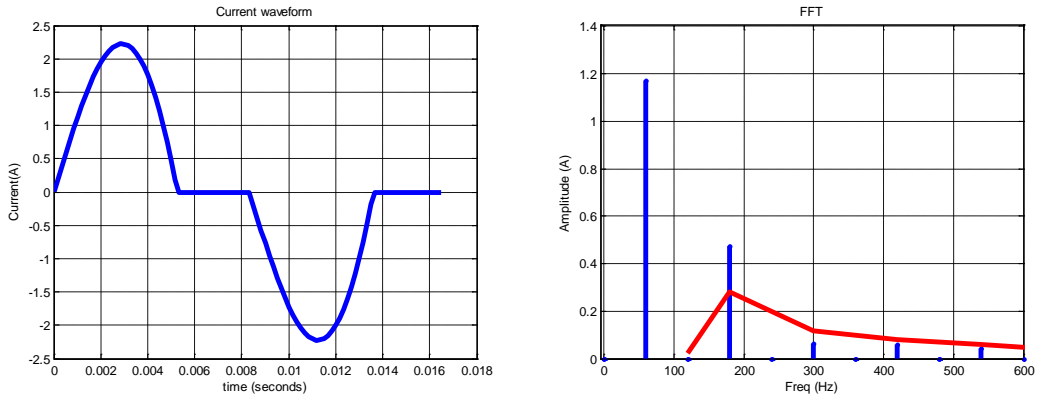


Fig. 17. Graphical representation of the theoretical distortion caused by the drive signal with uncompensated delays. Case studied $\Delta t_{on-off} = 40$ ns and $\Delta t_{off-on} = 80$ ns

Fig. 18 shows the same study for the case of $\Delta t_{on-off} = 80$ ns and $\Delta t_{off-on} = 40$ ns. The result is a power factor $PF = 0.945$ and total harmonic distortion THDi = 26.7%

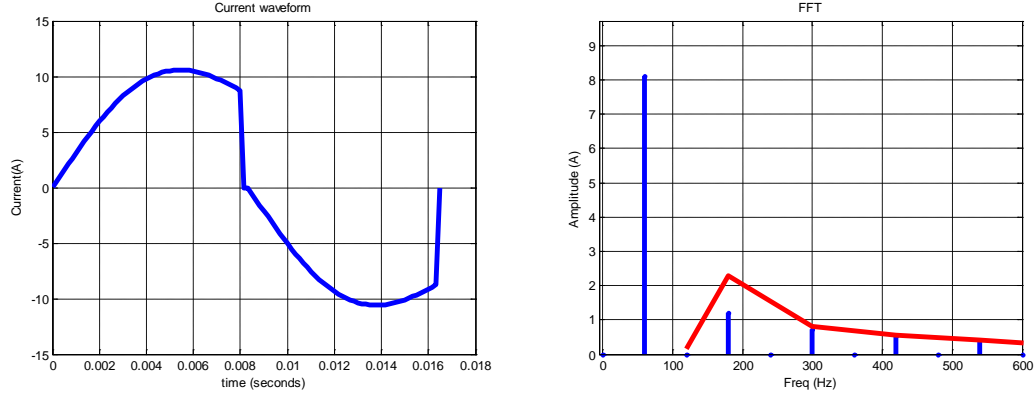


Fig. 18. Graphical representation of the theoretical distortion caused by the drive signal with uncompensated delays. Case studied $\Delta t_{\text{on-off}} = 80\text{ns}$ and $\Delta t_{\text{off-on}} = 40\text{ ns}$

The 10 ns resolution of the control algorithm is valid to obtain results under the EN-61000-3-2 class C limits.

APPENDIX II. CONTRIBUTION OF THE OUTPUT VOLTAGE RIPPLE TO THE CURRENT DISTORTION

Equation (3) is rewritten considering an output voltage ripple amplitude ΔV_o and ideal phase shift

$$V_m \frac{\hat{V}_{in} \sin(\omega t)}{V_o - \Delta V_o \sin(2\omega t)} = r_s i_{Lpk} \quad (13)$$

The input current has been evaluated with (13) against the EN-61000-3-2 class C limits using the $V_g = 120\text{V}$, 60 Hz case for $\Delta V_o/V_o = 10$ and 30%. Results are shown in Figs. 19 and 20 respectively. A PF = 0.998 is calculated for the 10% ripple and PF = 0.985 for the 30% ripple.

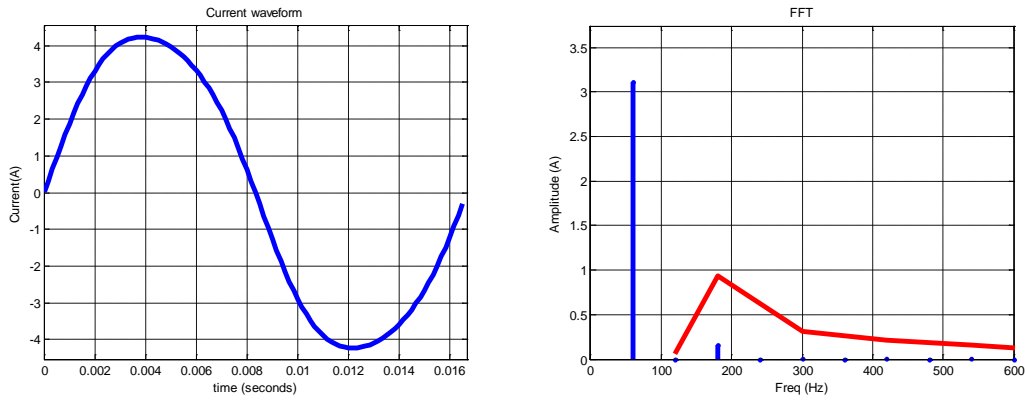


Fig. 19. Theoretical input current distortion caused by the output voltage ripple $\Delta V_o/V_o = 10\%$

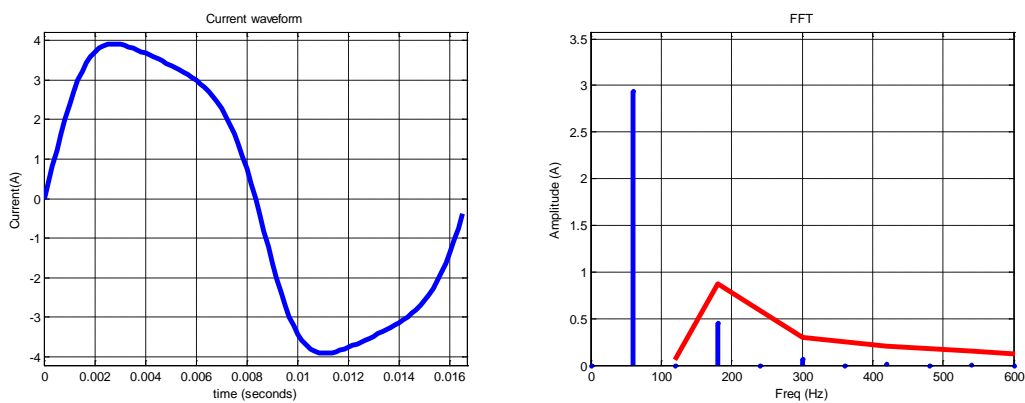


Fig. 20. Theoretical input current distortion caused by the output voltage ripple $\Delta V_o/V_o = 30\%$

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