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# **Towards lateral dots on few-layer transition metal dichalcogenides.**

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# Towards lateral dots on few-layer transition metal dichalcogenides (TMDCs)

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## Abstract

Owing to their unique properties, two-dimensional materials are a field of intense research activity since the discovery of graphene in 2004 [1]. Among these, semiconductor transition metal dichalcogenides (TMDCs) are of interest for applications that require a bandgap, such as field-effect transistors or quantum dots (QDs). Interestingly, theoretical work suggests that TMDC QDs have potential as an active element in quantum technologies, e. g. as valley filters or spin-valley qubits [2]. However, the experimental realization of controllable QDs in these materials still remains as a challenge. This project ultimately aims to contribute in this direction by experimentally realizing electrically tunable QDs in TMDCs. In this work, we take the first steps towards this goal. On the one hand, we start developing the technology to fabricate the envisioned devices. Parallely, we direct efforts towards optimizing the device geometry by means of electrostatic simulations using the software COMSOL Multiphysics [3]. In particular, we address the impacts of the gate geometry and of the thicknesses of the different 2D materials. We conclude that these two parameters are crucial in order to confine quantum dots with small enough dimensions to ensure a quantized energy spectrum. We also report on the experimental progress obtained with respect to the fabrication of TMDC devices.

## 1 Introduction

Two-dimensional materials are considered potential candidates for next-generation nanodevices owing to their interesting properties [4] [5]. In this family, graphene is the most studied material, due to its rich physics and high carrier mobility. However, for some applications such as e.g., field-effect transistors (FETs) and spin transistors, the lack of a bandgap and spin-orbit coupling limits the performance of graphene-based devices. Previous work has shown that these can be artificially induced in graphene, but it typically comprises carrier mobility, and can modify other material properties [6]. Hence, significant effort has been directed towards finding alternative two-dimensional materials. Semiconductor transition metal dichalcogenides (TMDCs) have emerged as a promising family of 2D materials due to their bandgap (ranging from 1 to 2 eV) [7] [8], which is dependent on the number of layers, and strong spin-orbit interaction. These properties make them potential candidates for electronic [9], spintronic [10] [11], and valleytronic [12] [13] applications.

In recent years, there has been a growing interest in the transport properties of semiconductor TMDCs,

which, in spite of their fascinating properties, have not been explored to the extent of graphene. Owing to their bandgap, 2D semiconductor devices with improved performance (e.g., field-effect transistors) have been demonstrated [9] [14]. Among the semiconductor TMDCs, MoS<sub>2</sub> is probably the most studied material because of its high availability in nature. Studies on other TMDC semiconductors are relatively scarce, even though it is expected that they can bring different device functionalities. For example, previous experimental work has reported on the ambipolar behavior of WSe<sub>2</sub> flakes [15].

Furthermore, the bandgap in semiconductor TMDCs paves the way towards the lateral confinement of low-dimensional structures by electrostatic gating, which has been a major challenge in graphene-based devices. In particular, the confinement of quantum dots in 2D materials is of interest due to potential applications in quantum technologies where the spin and valley degrees of freedom could be used for quantum computation [2]. Recently, a few experiments have demonstrated Coulomb blockade effects in TMDC-based devices [16] [17]. However, these studies have not shown evidence of the spin or valley degrees of freedom in the electron states presumably due to the excessive size of the confined dots.

Therefore, as a whole, the experimental demonstration of quantized states in few-layer TMDCs by electron transport is still lacking. It is noteworthy that, as a longer term objective, the demonstration of a spin-valley qubit based on 2D TMDC flakes would require the realization of a double quantum dot, which is a device geometry that enables to readout the electron spin via a charge measurement. To this end, it is also crucial to demonstrate electrostatic control over the coupling of neighboring quantum dots.

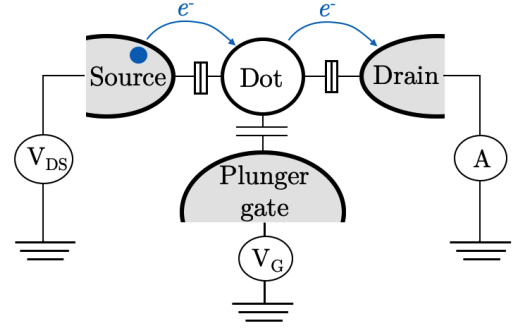
This master thesis is motivated by the prospects of realizing quantum dots on few-layer TMDCs (MoS<sub>2</sub> and WSe<sub>2</sub>) and of studying their rich underlying physics by electron transport. The first part of the thesis was dedicated to the experimental development of the technology to fabricate devices based on 2D materials, including the exfoliation of van der Waals heterostructures and the optimization of electrical contacts. In the second part, due to the exceptional circumstances experienced this year, our efforts were redirected towards optimizing the device geometry in order to maximize the chances to successfully accomplish our experimental goals. To this end, we have performed electrostatic simulations in order to uncover favorable device parameters for confining quantum dots with truly quantized energy spectrum in few-layer TMDCs. We have studied different gate geometries, differences between top or bottom gate configurations and the effect of the 2D material thickness. For this purpose, we have used a scientific simulation software (COMSOL Multiphysics [3]) to reproduce different gates designs and structures. After briefly explaining the theory behind QDs and introducing the corresponding modules of the software, we present the results for the different device geometries, as well as their advantages and drawbacks. We also report on the experimental progress obtained with respect to device fabrication.

## 2 Quantum dots (QDs)

A quantum dot is a zero-dimensional, artificially-structured system that displays a discrete energy spectrum owing to spatial confinement. Semiconductor quantum dots typically have a size of the order of 100 nm, and their discrete energy states can be occupied by either electrons or holes, depending whether the material is n-type or p-type.

Electron transport through QDs can be understood by considering a geometry in which the dot is coupled to source and drain contacts through tunnel junctions and capacitively to one or more gate electrodes (Figure 1). When the resistance of the tunnel junctions is large compared to the quantum resistance, the QD is in a regime known as Coulomb blockade (as will be discussed in more detail below).

In the Coulomb blockade regime, the number of charge



**Figure 1:** Schematic representation of a quantum dot system with an island where the dot resides (represented as a circle) coupled to source and drain contacts and a plunger gate.

carriers in the dot is a fixed integer  $N$ . It can be controlled by tuning the chemical potential of the dot via a so-called plunger gate<sup>1</sup>. Each  $N$ -electron charge state has a ground state and a series of excited states. A particular quantum state  $(N, n)$  is thus characterized by the energy  $E_N^{(n)}$ , where  $n = 0$  refers to the ground state, while  $n \geq 1$  corresponds to the excited states.

The electronic levels in the source (drain) contact are filled from the bottom of the conduction band up to the electrochemical potential  $\mu_S$  ( $\mu_D$ ). To better understand transport in Coulomb blockade, it is convenient to define the electrochemical potential of the QD, which describes the energy necessary to add an electron to the dot. For example, in a QD with initially  $N - 1$  electrons, the electrochemical potential for adding the  $N$ th electron is:

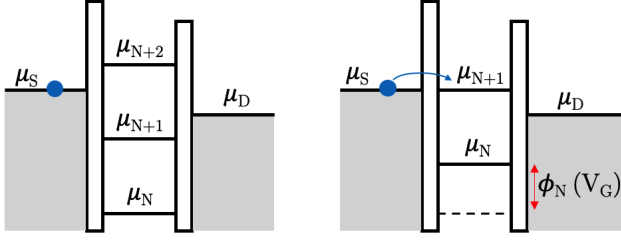
$$\mu_N(V_G) = E_N^{(0)}(V_G) - E_{N-1}^{(0)}(V_G) \quad (1)$$

Importantly,  $\mu_N$  varies linearly with the plunger gate voltage,  $V_G$ .

From the above relation, it can be inferred that a finite amount of energy is needed to add an electron to the quantum dot. This energy is called addition energy  $E_{add}$  and is composed of two different terms. The first term, known as charging energy,  $E_C$ , is an electrostatic term related to the Coulomb repulsion between electrons in the dot. It depends on the total capacitance of the dot,  $C_{dot}$  with respect to the electrodes. The second term is chemical, referring to the separation between quantized energy levels,  $\Delta\epsilon$ .

Coulomb blockade is lifted, i.e. electron transport can take place, whenever  $\mu_N(V_G)$  is inside the bias window defined by  $eV_{SD} = \mu_S - \mu_D$ , where  $e$  is the electron charge and  $V_{SD}$  is the voltage applied between source and drain. When this occurs, a single electron tunnels sequentially from the source contact to the dot and then from the dot to the drain contact. In this process, the transfer of a second electron to the dot is suppressed at

<sup>1</sup>From now on, we will refer to electrons even though it could be applied to electrons or holes



**Figure 2:** Energy level structure of a QD system in Coulomb blockade (left) and energy levels position where a current can flow between source and drain if a small bias voltage is applied (right).

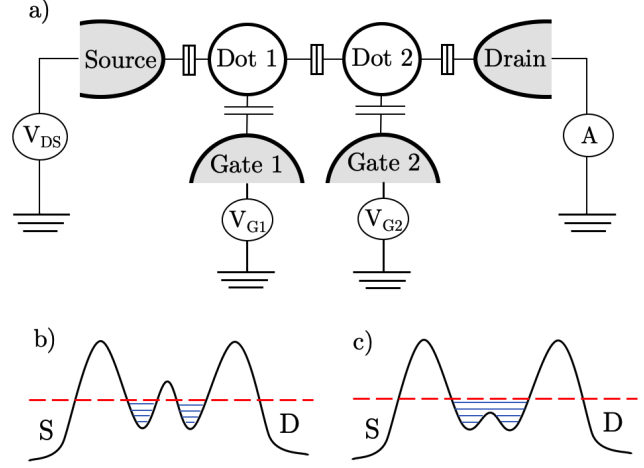
low  $V_{SD}$  by the charging energy. As the plunger gate voltage shifts  $\mu_N$  linearly, the QD conductance shows sharp resonances as a function of  $V_G$  for  $V_{SD} = 0$ , corresponding to charge transitions in which  $\mu_N$  is aligned with  $\mu_S$  and  $\mu_D$  [18]. At each of these transitions, the charge occupancy of the dot changes by one. The zero conductance valleys between Coulomb peaks correspond to the Coulomb blockade regime, in which transport is blocked. Both cases are schematically represented in Figure 2.

This remarkable effect allows to confine few electrons in QDs in a controllable, electrostatic way, paving the way for a number of applications. For example, recent work has demonstrated that the spin degree of freedom of single electrons or holes can be used as a quantum bit (the so-called spin qubits) [19] [20] [21].

The previous discussion addressed single quantum dots but coupled QDs (double and triple) can be understood in a similar way by considering the electrostatics of devices with a geometry that allows for controlling the electrochemical potential of each independent dot, as well as the interdot tunnel coupling. Individual quantum dots can be mutually coupled by making their separation very small. As a consequence of this small separation, interactions between neighboring gates have to be considered. Besides, the interdot coupling can also be tuned electrostatically with additional gates. In Figure 3, an example of two QDs in series is shown. This will be one of the arrangements used in our simulations.

### 3 COMSOL Multiphysics

COMSOL Multiphysics is an interactive simulation environment for modeling and solving numerous scientific and engineering problems. It includes a graphic Model Builder that allows the user to reproduce the design and geometry of the problem. One advantage of this software is that the models can be built by defining the relevant physical quantities, such as material properties and boundary conditions rather than by defining the underlying equations (usually partial differential equations,



**Figure 3:** a) Schematic arrangement of two quantum dots connected in series and placed between a source and a drain contact. Gate 1 (2) allows to control the number of electrons in the Dot 1 (2). b) and c) Energy landscapes of the system when varying the interdot coupling, going from two coupled QDs to a single QD. The red dotted line represents the Fermi energy of the system.

PDEs). The COMSOL Multiphysics software then internally compiles a set of equations representing the entire model and solves it using the Finite Element Method.

It contains several modules, corresponding to different physics interfaces, with nodes and settings that set up the equations and variables. For the purpose of this work, we used the AC/DC Module (Electromagnetics); in particular, the Electrostatics Interface.

#### 3.1 The AC/DC Module

The problem of electromagnetic analysis on a macroscopic level requires solving Maxwell's equations under certain boundary conditions. This can be done with the AC/DC Module.

Maxwell's equations are a set of equations stating the relationships between the fundamental electromagnetic quantities. For general time-varying fields, Maxwell's equations can be written as:

$$\nabla \times \mathbf{H} = \mathbf{J} + \frac{\partial \mathbf{D}}{\partial t} \quad (2)$$

$$\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t} \quad (3)$$

$$\nabla \cdot \mathbf{D} = \rho \quad (4)$$

$$\nabla \cdot \mathbf{B} = 0 \quad (5)$$

where  $\mathbf{J}$  is the current density,  $\mathbf{D}$  is the displacement field,  $\mathbf{E}$  is the electric field,  $\mathbf{B}$  is the magnetic flux density,  $\mathbf{H}$  is the magnetic field strength and  $\rho$  is the charge density [22].

Eq. 2 is also known as Ampère's-Maxwell law while Eq. 3 is known as Faraday's law. Besides, Eq. 4 and 5 correspond to two forms of Gauss' law: the magnetic and electric form, respectively.

Moreover, to obtain a closed system, it is necessary to include constitutive relations that describe the macroscopic properties of the medium.

### 3.2 The electrostatics interface

Electrostatics is the subfield of the electromagnetism describing an electric field caused by static charges.

The Electrostatics interface of COMSOL solves a charge conservation equation for the electric potential given the spatial distribution of the electric charge. The software carries out the modeling of static electric fields using the electric potential  $V$ . By combining the definition of potential with Gauss' law (Eq. 5) and the corresponding constitutive relation, it is possible to derive the classic Poisson's equation [22].

As the scope of this project is the study of stationary electric fields, the applicable constitutive relation is the one relating the electric polarization vector  $\mathbf{P}$ , the displacement field  $\mathbf{D}$  and the electric field  $\mathbf{E}$  as follows:

$$\mathbf{D} = \varepsilon_0 \varepsilon_r \mathbf{E} + \mathbf{P} \quad (6)$$

where  $\varepsilon_0$  and  $\varepsilon_r$  are the vacuum permittivity and the relative permittivity of the material respectively.  $\mathbf{P}$  describes how the material is polarized when an electric field is present. It can be interpreted as the volume density of electric dipole moments.

Under static conditions, the electric potential,  $V$ , is defined by the relationship  $\mathbf{E} = -\nabla V$ . Combining this expression with Eq. 6, the aforementioned Poisson's equation is obtained:

$$-\nabla \cdot (\varepsilon_0 \varepsilon_r \nabla V - \mathbf{P}) = \rho \quad (7)$$

If the material has no net polarization,  $\mathbf{P} = 0$ . Hence,

$$\nabla^2 V = -\frac{\rho}{\varepsilon_0 \varepsilon_r} \quad (8)$$

This equation describes the electrostatic field in dielectric materials. When there is no space charge ( $\rho_s = 0$ ), Poisson's equation becomes Laplace's equation:

$$\nabla^2 V = 0 \quad (9)$$

On the other hand, as mentioned before, to get a full description of an electromagnetic problem, boundary conditions must be specified at material interfaces and physical boundaries. The relevant interface condition at interfaces between different media for our case is:

$$\mathbf{n}_2 \cdot (\mathbf{D}_1 - \mathbf{D}_2) = \rho_s \quad (10)$$

where  $\rho_s$  denotes surface charge density and  $\mathbf{n}_2$  is the outward normal from medium. In the absence of surface charges, this condition is fulfilled by the boundary condition [22]:

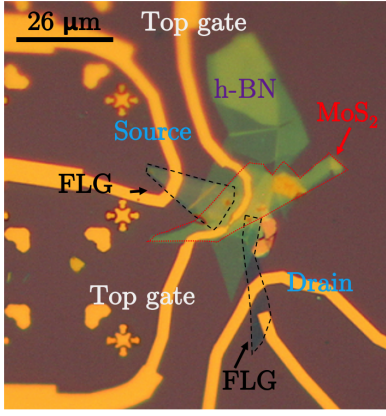
$$\begin{aligned} \mathbf{n} \cdot [(\varepsilon_0 \varepsilon_r \nabla V - \mathbf{P})_1 - (\varepsilon_0 \varepsilon_r \nabla V - \mathbf{P})_2] &= -\mathbf{n} \cdot (\mathbf{D}_1 - \mathbf{D}_2) \\ &= 0 \end{aligned} \quad (11)$$

## 4 Methods

Here, we address some of the challenges towards the main goal of this project, which is to experimentally realize lateral quantum dots on gated few-layer TMDCs. On the one hand, we have started developing the technology to fabricate devices based on thin TMDC flakes encapsulated by boron nitride and with local gate electrodes. In parallel, we have studied the optimal gate geometry for confining small quantum dots in TMDCs by means of electrostatic simulations.

### 4.1 Sample fabrication

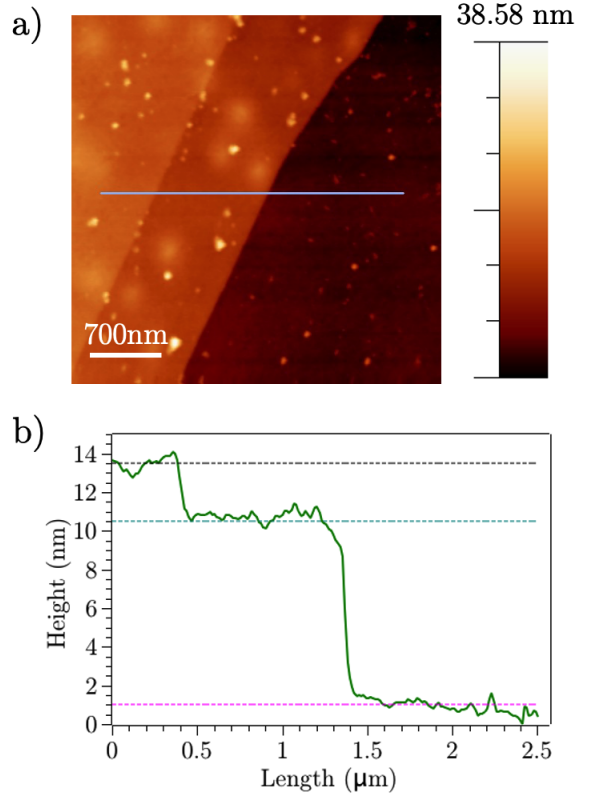
Our sample preparation method for the experiments is based on the exfoliation of MoS<sub>2</sub> or WSe<sub>2</sub> flakes by micromechanical cleavage (also commonly known as the *scotch tape* method). Exfoliated flakes are subsequently transferred by all-dry transfer mediated by polydimethylsiloxane (PDMS) films onto highly n-doped Si substrates (5 × 5 mm) covered by a 300 nm SiO<sub>2</sub> layer. In our experiments, the degenerately doped Si is employed as a global backgate. The substrates are prepatterned with bottom gate structures, which consist of approximately 35-nm wide Cr/Au (2.5 nm/10 nm) lines. Hexagonal boron-nitride (hBN) is used as a dielectric between the bottom gates and the TMDC flake. In a previous study, we have shown that electrical switches resulting from charge impurities on the Si/SiO<sub>2</sub> substrate can be greatly minimized by employing hBN dielectrics to isolate the TMDC flake. Ideally, the flake should be fully encapsulated for a better isolation from charge perturbations and thus, for an improved performance. The device nanofabrication starts by designing the desired geometry with the software KLayout [23]. The designed pattern is transferred to the actual sample via e-beam lithography, followed by the evaporation of Cr/Au (5 nm/100 nm) contacts and standard lift-off techniques. As a way to minimize the contact resistance, we use few-layer-graphite (FLG) flakes as the contacts to the TMDC flake. We note here that the graphite-based contacts are not explicitly taken into account in our electrostatic simulations as they are sufficiently far from the region where the quantum dots are confined. An image of a finished device is presented in Figure 4.



**Figure 4:** Optical microscope image of a MoS<sub>2</sub> flake top-encapsulated with hBN, top gates and FLG contacts.

We estimate (by the optical contrast in a microscope) that the thickness of our exfoliated MoS<sub>2</sub>, WSe<sub>2</sub> and hBN flakes falls within a range of 5-30 nm. We have found that flakes thinner than 5 nm (which is approximately equivalent to 7 layers for MoS<sub>2</sub> and WSe<sub>2</sub> [24] and 14 layers for hBN [25]) are relatively difficult to obtain with the above exfoliation procedure. Further optimization will be carried out for future studies directed at the investigation of monolayer TMDC devices. On the other hand, we considered flakes thicker than 30 nm as bulk. We note that, while optical contrast is not the most accurate method for quantifying the thickness of 2D materials, it is commonly used as a quick way to identify thin flakes [26]. For a precise quantification of the flake thickness, techniques such as atomic force microscopy (AFM) or Raman spectroscopy are required.

To evaluate whether our thickness estimation by optical contrast is reliable, we have performed AFM characterization on two different flakes (one of hBN and another of MoS<sub>2</sub>). We have used WSxM [27] and Gwyddion [28] softwares for image acquisition and post processing, including the extraction of the height profiles. Figure 5 displays an AFM topography image of an hBN flake where two thin steps are visible, as underscored by the line cut in panel b)); their heights are, approximately, 9.5 nm and 12.5 nm respectively, i.e. within the range we estimate from the optical images. For the MoS<sub>2</sub> sample, we have selected a flake that could be considered mainly as bulk by the optical contrast (i.e., thickness larger than 30 nm), but that also had a smaller region with reduced thickness. The corresponding AFM image, shown in Figure 6, reveals that the thinner area has a height of  $\approx 5.5$  nm, whereas the bulk region has a thickness of  $\approx 24$  nm, again in good agreement with our previous assessment. Note that these measurements have an offset of  $\approx 1$  nm. In summary, we conclude that the thickness values obtained by AFM are in relative good agreement with our estimations by optical contrast. Therefore, we have opted to employ the optical characterization as a



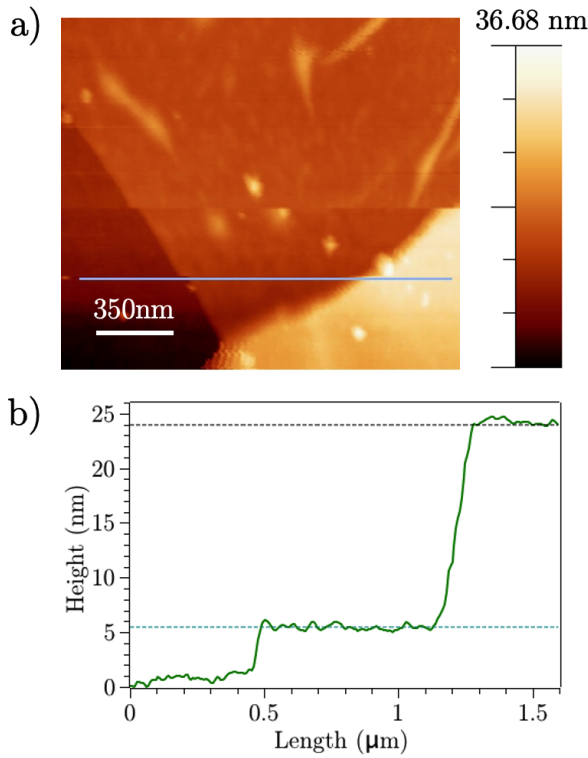
**Figure 5:** a) AFM image of an hBN flake of different thicknesses (lighter regions) on a Si/SiO<sub>2</sub> substrate (dark region). The bright dots are dirt on the sample. The blue horizontal line indicates where the height profile is taken. b) Height profile of the sample where two different height steps can be seen; blue ( $\approx 10.5$  nm) and black ( $\approx 13.5$  nm) dashed lines are a guide to the eye of the average thickness of these steps whereas the pink dashed line is the reference of the substrate ( $\approx 1$  nm).

means to quickly identify thin flakes for our devices. For future studies centered at monolayer and bilayer flakes, however, it will be crucial to also characterize the samples by AFM or Raman spectroscopy.

Since it is difficult to precisely determine the number of layers in a given flake during the exfoliation process, in this work, we have fabricated devices using TMDC and hBN flakes of different thicknesses (within the range 5-30 nm, as discussed above). For this reason, we have decided to also investigate the effects of the thickness of the flakes in our electrostatic simulations.

## 4.2 Simulations

In this work, we have performed electrostatic simulations to study the optimal device geometry to confine lateral quantum dots in few-layer TMDCs. The main objective was to search favorable parameters for the confinement of small quantum dots (i.e., with a radius smaller than approximately 100 nm, to ensure a quantized energy spectrum measurable at low temperatures [2]). To this end,

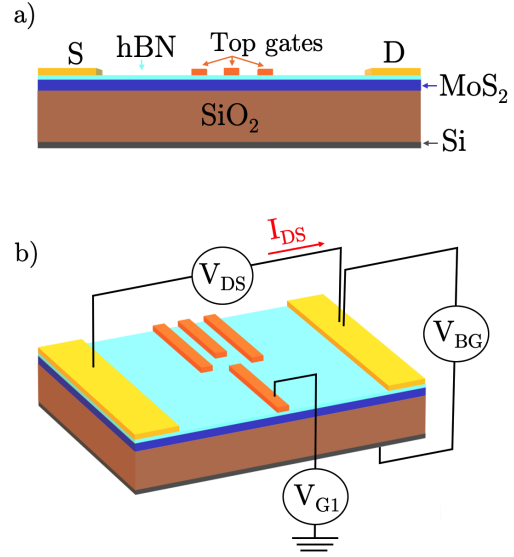


**Figure 6:** a) AFM image of a MoS<sub>2</sub> flake of different thicknesses (lighter regions) on a Si/SiO<sub>2</sub> substrate (dark region). The bright dots are dirt on the sample and the mismatch of the image in the middle region of the image is due to a jump of the AFM tip during the measurements. The blue horizontal line indicates where the height profile is taken. b) Height profile of the sample where two different height steps can be seen; blue ( $\approx 5.5$  nm) and black ( $\approx 24$  nm) dashed lines are a guide to the eye of the average thickness of these steps. The reference here is set at  $\approx 0$  nm.

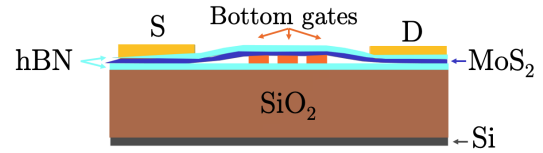
we study two different arrangements of the gates, top gates (Figure 7) and bottom gates (Figure 8), as well as the effect of the spatial dimensions of the gates.

Three-terminal devices based on TMDC flakes behave as Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs): the conductivity in the channel between source and drain contacts is controlled by a gate. Indeed, these devices can switch between so-called *off* and *on* states: in the *on* state, the channel has a low resistance and a high on-current can flow through it. In the *off* state, the resistance is high and just a small off-current flows through it. The gate voltage for which the transistor switches from *off* to *on* is called threshold voltage,  $V_{th}$ . The above behavior can be captured in a simple electrostatic model based on a capacitor, in which the charge in the channel is equal to  $C \cdot (V_G - V_{th})$ , where  $V_G$  is the voltage applied to the gate and  $C$  is the gate-flake capacitance. We consider that the flake is uncharged for gate voltages below  $V_{th}$ .

In this work, we study devices with more complex geometries. Apart from a global gate used to charge the



**Figure 7:** a) Scheme of a MoS<sub>2</sub> device with top gates and b) scheme of the electrical circuit for the transport measurements. For simplicity here, only one top gate is connected. Note that drawing is not to scale.



**Figure 8:** a) Scheme of a MoS<sub>2</sub> device fully encapsulated with hBN and bottom gates. Note that drawing is not to scale.

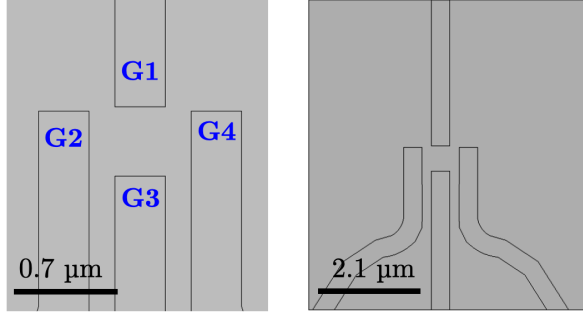
TMDC flake, we employ local gates depletion to create tunnel barriers and confine quantum dots. To simulate the formation of QDs, we study the electrostatic potential induced on the TMDC flake. Similar to the model above, we consider that charges accumulate in the TMDC only when the induced potential is higher than  $V_{th}$  (which we take to be equal to zero).

The simplified workflow in COMSOL is the following: firstly, it is necessary to define the relevant parameters for the materials (namely, the relative permittivity, the thickness of a 2D monolayer and the number of layers). Secondly, we import the gate design and, from this element, we build the whole 3D geometry, similar to the real devices used in our experiments. The different regions (so-called domains) in the device are assigned to each specific corresponding material. After that, we define the electrostatic boundary conditions, including the voltage range applied to the gates in the study. Lastly, the built-in FEM solver in COMSOL is invoked to solve the PDE problem. A more detailed technical description of the process to setup the simulations can be found in the Appendix C.

Through the simulations, we will try to clarify: (i) the role of the thickness of the gate dielectrics (hBN) and the semiconductor TMDC flakes ( $\text{MoS}_2$  or  $\text{WSe}_2$ ) on the confinement of quantum dots, (ii) whether there are advantages in employing top-gate or bottom-gate structures and (iii) the most suitable gate geometry (size and arrangement) for our purposes. To this end, we have studied seven different device structures.

The first three geometries are intended to study the confinement of a single quantum dot by means of four local gates. The main differences between these geometries is the width of the electrodes and whether the gates are located on top or in the bottom of the flake (top gates/bottom gates).

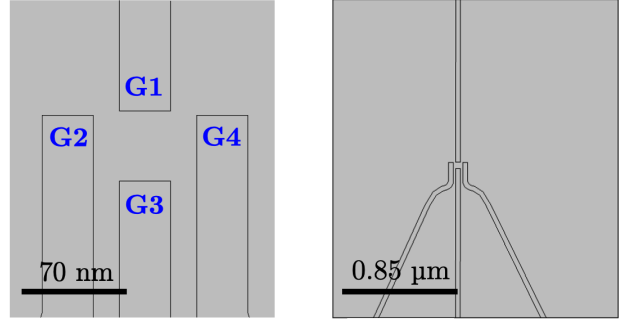
- I)**  $\text{MoS}_2$  device with top gates (Figure 9). In this case, the flake was first top-encapsulated with hBN (schematic representation in Figure 7) and, for comparison, fully-encapsulated later (see Appendix B).



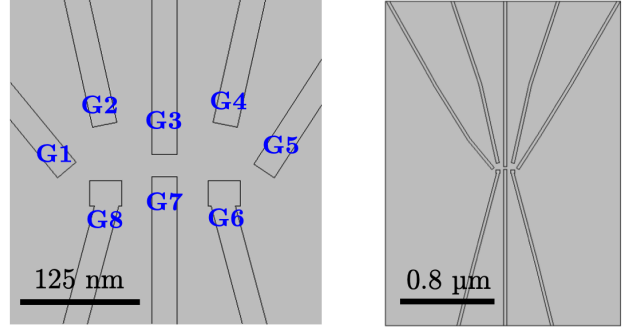
**Figure 9:** Zoom in (left) and top view (right) of the gates design corresponding to the structure described in **I**). We have used this design for some devices experimentally. G1-G4 correspond to the gate number.

- II)**  $\text{MoS}_2$  device with bottom gates with the same geometry as **I**). In this instance, we bottom-encapsulated the flake firstly and fully encapsulated (see Appendix B) afterwards (Figure 8).

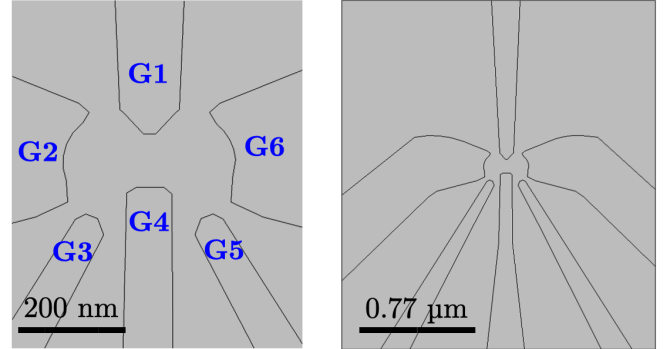
- III)**  $\text{MoS}_2$  device with same configuration as **I**) but thinner gates (Figure 10).



**Figure 10:** Zoom in (left) and top view (right) of the gates design corresponding to the structure described in **III**). G1-G4 correspond to the gate number.



**Figure 11:** Zoom in (left) and top view (right) of the gates design corresponding to the structure described in **IV**). This is the standard design for our transport experiments. G1-G8 correspond to the gate number.



**Figure 12:** Zoom in (left) and top view (right) of the gates design corresponding to the structure described in **V**). G1-G6 correspond to the gate number.

The last four geometries are used to investigate the confinement of double QDs. The main differences here are the gate design (shape, width and arrangement) and the number of gate electrodes:

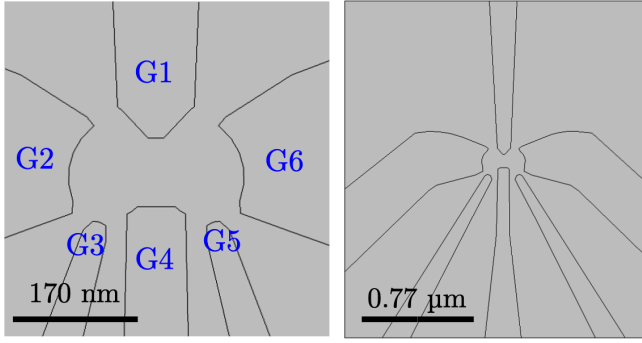
- IV)**  $\text{MoS}_2$  device with bottom gates whose design has been used in our previous experiments (Figure 11).

- V)**  $\text{MoS}_2$  device with bottom gates, design based on [29] (Figure 12) for comparison with our actual design. We wanted to see whether we could make an improvement modifying our design.

- VI)**  $\text{MoS}_2$  device with bottom gates, design based on [29] with slight modifications in order to get better results (i.e., smaller QDs) .

- VII)** Same as **V**) but using  $\text{WSe}_2$  as the semiconductor flake. For these results, see Appendix A.

Preliminary electrostatic simulations were performed in order to evaluate the effect of the source and drain electrodes, which were connected to ground, on the induced electrostatic potential in the flake [30]. We verified that, owing to the distance between the electrical leads



**Figure 13:** Zoom in (left) and top view (right) of the gates design corresponding to the structure described in **VI**. G1-G6 correspond to the gate number.

and the area of interest (which is approximately  $3 \mu\text{m}$  in our real devices), their effect is negligible. As a result, all simulations discussed below were carried out using geometries without source and drain contacts and where the TMDC flake is kept floating. Our methodology is similar to those employed in previous works reporting electrostatic simulations of QDs on TMDCs [16] [29]. In the discussion below, we compare our results with those reported in these references and analyze possible improvements that can be done.

## 5 Results

### 5.1 Experimental results

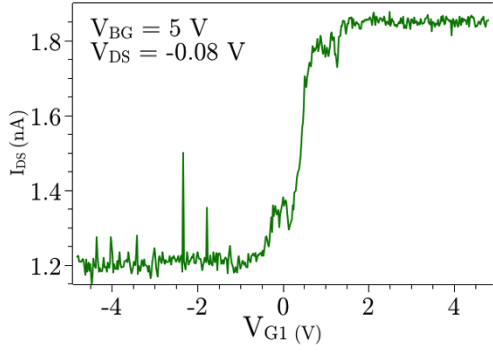
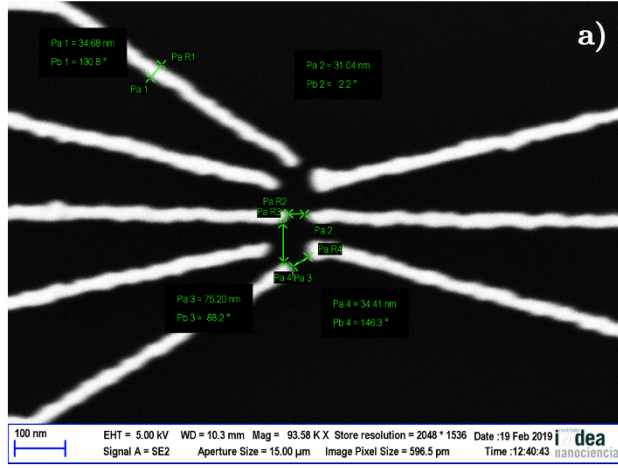
During the first part of this project, we have focused on the fabrication of few-layer  $\text{MoS}_2$  devices fully encapsulated by hBN flakes and contacted by FLG electrical leads. The devices also incorporated local gates for confining quantum dots at a later step. In most of the samples, we have employed the bottom gate geometry shown in Figure 14 a), which was intended for the confinement of double QDs. We note that, at that time, this gate design had not been optimized by electrostatic simulations, but rather was adopted to test the limits of our nano-fabrication. As we will discuss later, the simulations performed in the second part of this work indicate that this gate geometry might not be ideal for confining double dots. In addition, we have also experimented with a top gate geometry in a few samples. Top gates, however, present a few practical disadvantages: (1) a specific gate design is required for each sample to ensure that the gates are aligned with the  $\text{MoS}_2$  flake, (2) the fabrication requires an additional step of e-beam lithography, evaporation and lift-off, and (3) the electrical connection from the gates to the bonding pads might be interrupted at the edges of the van der Waals heterostructures (very thin gates require a reduced metallization thickness).

Once the fabrication of the samples is finished, we first test the devices in a probe station at room tempera-

ture. To this end, we employ the degenerately-doped Si in the back side of the chip as a global gate and measure the current flowing through the  $\text{MoS}_2$  flake. During this measurement, all other local gates are kept floating. This initial characterization is useful to verify whether the fabrication was successful. A typical field effect curve is shown in Figure 15, where the current,  $I$ , at a constant source-drain bias  $V_{DS} = 30 \text{ mV}$  is plotted against the back gate voltage. The resistance measured at  $V_{BG} = 10 \text{ V}$  is  $\approx 6 \text{ M}\Omega$ . Although it is possible to infer from the trend of the curve that the resistance would still decrease with increasing gate voltage, the measured values are much higher (up to two orders of magnitude) than those reported in similar experiments in the literature [9]. In addition, from the curve above, we extract a device transconductance (defined as  $g_m = dI_{DS}/dV_{BG}$ ) of approximately  $0.02 \mu\text{S}$ , which is two orders of magnitude smaller than the best values found in the literature, and a field effect mobility (defined as  $\mu = [dI_{DS}/dV_{BG}] \times [L/(wC_iV_{DS})]$ , where  $L = 13.7 \mu\text{m}$  is the channel length,  $w = 8.5 \mu\text{m}$  is the channel width and  $C_i = 1.15 \times 10^{-4} \text{ Fm}^{-2}$  is the capacitance between the channel and the back gate per unit area) of  $\approx 80 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ , three times smaller than the one reported by ref. [9]. Possible reasons for the above discrepancies include the contact resistance or the relatively low capacitance of our global back gate [31]. To tackle this issue, we are currently trying to optimize our FLG contacts, while also experimenting with other methodologies for low contact resistance reported in the literature [32], and with the incorporation of graphite-based gates that are part of the van der Waals heterostructure.

In order to perform measurements at low temperature, the samples are wire-bonded to a printed-circuit board which is then connected to a 4.2 K insert. Preliminary measurements indicate that, although not yet fully optimized, the few-layer graphite contacts minimize the contact resistance in our devices sufficiently to allow transport to be measured down to 4.2 K (in previous devices with Au-based contacts, transport would freeze out at low temperatures). We have also verified that the bottom gates work at low temperatures as shown in Figure 14 b). Here we see that the drain current drops sharply with decreasing bottom gate voltage,  $V_{G1}$ , (starting at around 1 V) before stabilizing at a constant value for  $V_{G1} < -1 \text{ V}$ . We do not observe the current going down to zero because, in this device, not all local gates were working, presumably due to some problems in the electrical connection. As such, in this measurement, the electron gas is only depleted underneath one of the local gates which is not enough to turn the device to the off-state.

The above results indicate that we need to further improve our fabrication technology of TMDC devices (particularly, to reduce the contact resistance), but also that we already have the basic elements for performing the planned experiments, namely: (i) working electrical con-



**Figure 14:** a) SEM image (top view) of a real device with bottom gates for confining a double QD (design in Figure 11). As this image was used for other purposes different to this project, the parameters indicated are not relevant for this work b) Experimental field effect curve of a bottom gate at 8K

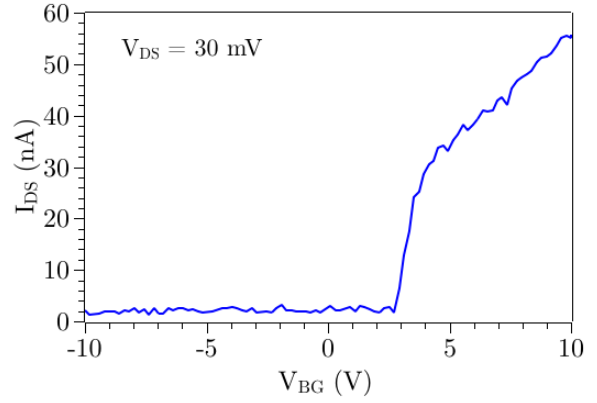
tacts at low temperature and (ii) working local gates. We have also recently prepared new samples that we expect to test at low temperature in the very near future. In the next subsections, we will discuss electrostatic simulations directed at optimizing the device geometry, which will be of importance in the preparation of our new generation of samples.

## 5.2 Simulations results

### 5.2.1 Single quantum dot

Similarly to our experiments, the devices in all of our simulations incorporate a global back gate that is kept at a fixed potential and whose function is to charge the TMDC flake. The barriers to confine quantum dots are created by the local gates that locally deplete this electron gas. As a starting point for this part of the work, we employ a simpler single quantum dot geometry to test our simulations, and to start studying the effect of some of the parameters in our devices.

We start with the top gate geometry shown in Fig-

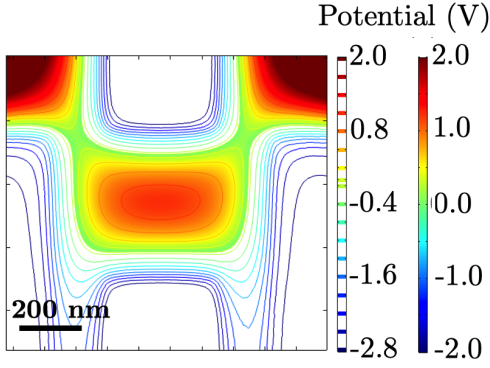


**Figure 15:** Experimental field effect curve of the source and drain contacts at ambient temperature.

ure 9, which was a gate design that we had previously tested experimentally. This design has only four local gates (gate width is 350 nm), three of them for controlling the coupling of the dot with the source and drain contacts and the fourth one, for changing the size of the dot and its charge occupancy. In this instance, the semiconductor flake was bottom-encapsulated with hBN, as it was explained in the previous section I). The simulations were carried out for different thicknesses of the hBN dielectric (5-30 nm) and of the MoS<sub>2</sub> flake (5nm and 20 nm).

With this geometry, we observe that quantum dots can be easily formed by tuning the voltages in the local gates, i.e. we find a large gate voltage parameter space for the confinement of dots. We also observe that the thicknesses of the hBN and TMDC flakes do not play an important role in this case. In addition, we observe that the size of the dot can be tuned electrostatically. An example of a QD confined in a 20 nm-thick MoS<sub>2</sub> flake encapsulated by a 20 nm-thick hBN flake is presented in Figure 16. In this plot, the dot appears as an island of positive induced potential connected to the electrical leads on the top left and right sides, while the barriers display a negative potential. We get dots that are not perfectly circular but rather rectangular-shaped with a size of approximately 100 nm × 600 nm (depending on the voltages applied to the gates). These values are a bit larger than those reported by Song et al. [16], who simulated the electrostatic confinement of dots in WSe<sub>2</sub>-based devices obtaining QD radii ranging from 275 to 150 nm. The discrepancy in size can be attributed to the narrower gates (200 nm) and to slight differences in the gate geometry used in that work. Importantly, the above QD dimensions are still too large to access the quantization of energy levels in these materials [2]. To address the possibility of confining truly quantized dots, we will later consider the case of a similar geometry but with narrower gate electrodes.

Before doing that, we first evaluate the differences be-



**Figure 16:** COMSOL simulation of the potential profile in 20 nm MoS<sub>2</sub> layer for the electrode pattern shown in Figure 9 as top gates for 20 nm of hBN. Here,  $V_{BG} = 6$  V,  $V_1 = -5$  V,  $V_2 = V_4 = -4$  V, and  $V_3 = -5$  V. The closed contours indicate where the quantum dot may be located.

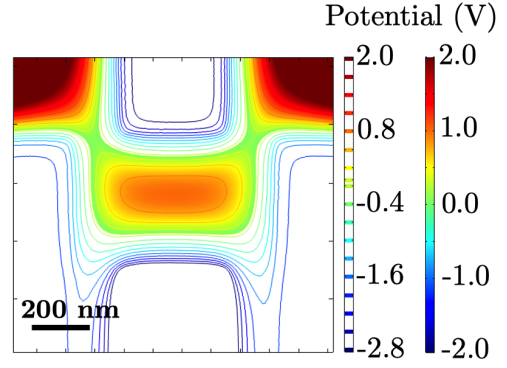
tween having the local gates placed on top or underneath the TMDC flake. One of the practical advantages of bottom gate geometries is the possibility of pre-fabricating multiple chips with local gates simultaneously. In addition, it is simpler to design devices with a standard gate geometry (as opposed to doing a specific design for each sample, for the case of top-gated devices) and it is not difficult to transfer the van der Waals heterostructure onto the pre-fabricated gates. Finally, it is easier to reduce the gate width without having problems related to discontinuities of the electrical connection between the bonding pads and the device, as discussed in II).

A first important difference of the bottom gate case is the fact that the local gates partially screen the global back gate (Figure 18) imparting a less homogeneous initial charging of the TMDC flake (e.g. when the local gates are fixed to 0 V, and a finite voltage is applied to the back gate). We observe that, nevertheless, it is also possible to confine QDs with bottom gates with a relatively large gate voltage parameter space. Again, the 2D material thickness seems to play a minor role in the dot confinement. In addition, these dots show very similar shapes and sizes as in the preceding geometry (Figure 17 as an example). We therefore conclude that overall, there is no clear advantage with respect to using a top or bottom gate configuration in relation to shrinking the size of the confined QDs. For this reason, we will adopt a bottom gate configuration for the following simulations, due to the benefits related to fabrication discussed above.

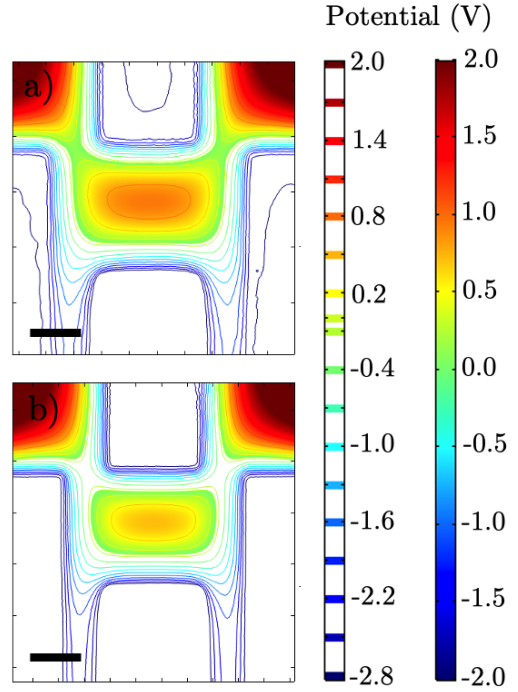
Moreover, in relation to the barrier height, both instances are comparable. This height ( $\approx 3$  eV) seems to be enough to confine a QD.

We now evaluate whether it is possible to shrink the size of confined QDs by employing a similar geometry as the one discussed above, but where we reduce the gate width to 35 nm (Figure 10), a value that is still experimentally achievable with our nanofabrication.

For this geometry, we observe that even though the

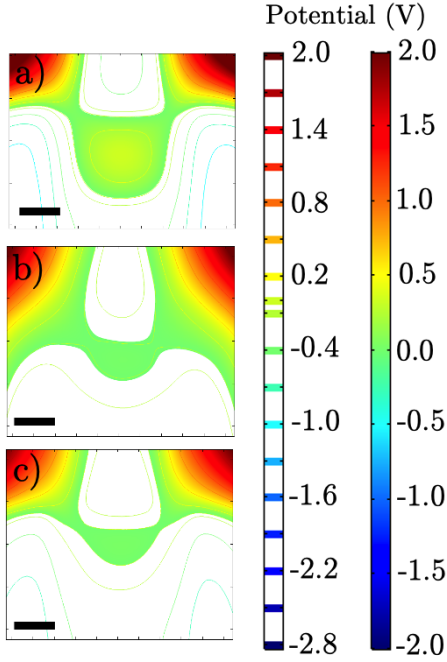


**Figure 17:** COMSOL simulation of the potential profile in a 20 nm MoS<sub>2</sub> layer for the electrode design shown in Figure 9 as bottom gates for 10 nm of hBN. Here,  $V_{BG} = 6$  V,  $V_1 = -3$  V,  $V_2 = V_4 = -2$  V,  $V_3 = -5$  V and  $V_4 = -2$  V. The closed contours indicate where the quantum dot may be located.



**Figure 18:** Simulation of the potential profile in a 5 nm MoS<sub>2</sub> layer and 5 nm of hBN for a) top gates and b) bottom gates with a scale bar of 200 nm. Here,  $V_{BG} = 4$  V,  $V_1 = -3$  V,  $V_2 = V_4 = -3$  V,  $V_3 = -5$  V. The effect of the screening of the bottom gates over the backgate can be seen in the coupling of the QD with the source and drain.

parameter space becomes constrained, the confinement of much smaller dots becomes possible. As an example, for the device shown in Figure 19 a) (thicknesses: 5nm MoS<sub>2</sub>, 20 nm hBN), we were able to obtain a QD with a radius of approximately 20 nm, which would be well inside the energy quantization limit. To achieve these small sizes, the thickness of the 2D materials (hBN and MoS<sub>2</sub>) starts playing a more important role. Indeed, while we could obtain well-defined quantum dots for certain gating conditions in devices with a 5 nm-thick MoS<sub>2</sub>

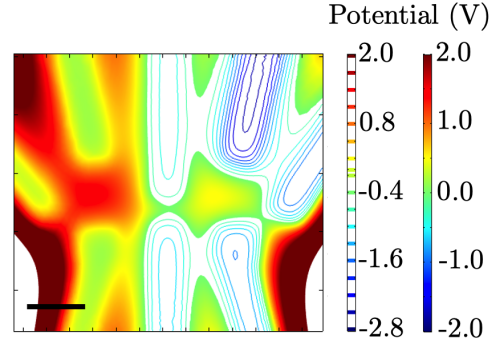


**Figure 19:** Simulation of the potential profile for the electrodes design shown in Figure 10 as bottom gates for different MoS<sub>2</sub> and hBN thicknesses: (a) 5 nm MoS<sub>2</sub> and 5 nm hBN; (b) 5 nm MoS<sub>2</sub> and 20 nm hBN; (c) 20 nm MoS<sub>2</sub> and 5 nm hBN with a scale bar of 200 nm. Here,  $V_{BG} = 15$  V for all the cases; a)  $V_1 = -0.7$  V,  $V_2 = -1.35$  V,  $V_3 = -0.3$  V and  $V_4 = -1.35$  V; b)  $V_1 = -1.3$  V,  $V_2 = -1.03$  V,  $V_3 = -0.2$  V and  $V_4 = -1.09$  V; c)  $V_1 = -0.8$  V,  $V_2 = -1.5$  V,  $V_3 = -0.2$  V and  $V_4 = -1.53$ . A QD is confined for very specific set of voltage values and thicknesses.

flake (Figure 19 a) and b), this turned out to be a lot more difficult when the MoS<sub>2</sub> thickness was increased to 20 nm (Figure 19 c). Similarly, we have observed that reducing the thickness of the hBN dielectric layer was beneficial for confining dots in this geometry. Overall, this latter effect is presumably linked to a stronger gate coupling resulting from the increased gate capacitance as the thickness of the dielectric layer decreases. We thus conclude that, to obtain smaller quantum dots, it is essential to reduce the hBN thickness.

### 5.2.2 Double quantum dot

We finally address gate geometries that would allow us to confine double QDs with tunable interdot coupling, which is the main goal of this project. We expect that the simulations will help to optimize our device geometry and fabrication. We start by studying the design presented in Figure 11, which is the same that we are currently using experimentally (as shown in Figure 14). It includes pairs of gates at the device extremities to enable control over the coupling between the dots and the source and drain contacts, two plunger gates to control the electrochemical potential of each dot and a pair



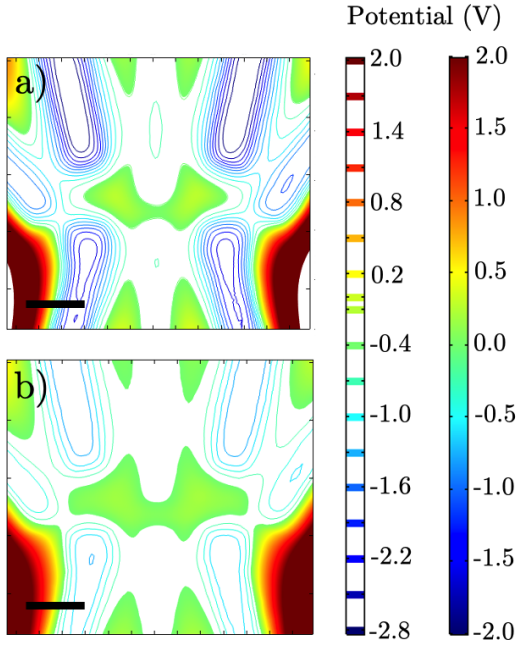
**Figure 20:** Simulation of the potential profile in the 5 nm MoS<sub>2</sub> layer for the electrode design of the device shown in Figure 11 as bottom gates for 5 nm of hBN with a scale bar of 50 nm. Here,  $V_{BG} = 20$  V,  $V_3 = -0.6$  V,  $V_4 = -2.1$  V,  $V_5 = -1.55$  V,  $V_6 = -1.25$  V,  $V_7 = -0.85$ . A single QD is formed.

of gates in the middle to tune the tunnel coupling between dots. In our experimental nano-fabrication, the gate width is limited by the resolution of the e-beam lithography process. We are able to reproducibly fabricate 35 nm-wide metal lines and thus, our simulations are carried out using gates with this width.

We start by trying to confined single QDs by employing a subset of the bottom gates. Figure 20 reveals that this can be accomplished, as evidenced by the QD connected to both electrical leads, even though the parameter space is limited. In this example, the unused local gates are kept at ground potential, which ends up heavily screening the voltage applied to the global back gate. This leads to a non-uniform charging of the TMDC electron gas and to the formation of local barriers (green regions on the left side of the sample), which complicates the confinement of the single dot. This problem can be circumvented, both in the simulations and in an experiment, by positively biasing the gates that are not used in the confinement.

Finally, we turn to simulations of double quantum dots. Overall, we find that, due to the large number of gate electrodes in the device geometry as well as to the close proximity of such gates, which leads to cross-talk, it becomes very difficult to confine small double dots coupled to the electrical leads and with interdot tunnel coupling. In Figure 21, we present two examples of confined double quantum dots that we were able to obtain for very specific values of gate voltages (the slight asymmetry between both dots is due to the small differences on the simulation mesh). In addition to such an extremely reduced parameter space, we observed that the coupling to the electrical leads (on the bottom left and right sides) is reduced and it was not possible to significantly increase it without affecting the dots.

The results of the above simulations indicate that our current gate geometry is not ideal for confining double quantum dots, mainly due to the cross-talk between



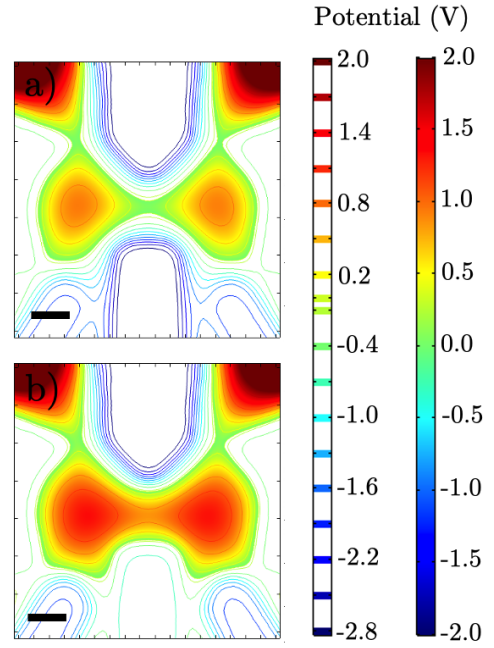
**Figure 21:** Simulation of the potential profile in the 5 nm (a) and 20 nm (b) MoS<sub>2</sub> layer for the electrode design of the device shown in Figure 10 as bottom gates for 5 nm hBN flake with a scale bar of 50 nm. Here,  $V_{BG} = 20$  V for both cases; a)  $V_1 = -1.5$  V,  $V_2 = -2.5$  V,  $V_3 = -0.25$  V,  $V_4 = -2.5$  V,  $V_5 = -1.5$  V,  $V_6 = -2$  V,  $V_7 = -0.25$  V,  $V_8 = -2$  V; b)  $V_1 = -1.5$  V,  $V_2 = -1.5$  V,  $V_3 = -0.25$  V,  $V_4 = -1.5$  V,  $V_5 = -1.5$  V,  $V_6 = -1.5$  V,  $V_7 = -0.25$  V,  $V_8 = -1.5$  V. No double dot with the appropriate coupling to the source and drain is formed using this geometry. Besides, it is not tunable into two single QDs with the gates.

nearby gates. Improvements to this design would require a rearrangement of the local gates.

### 5.2.3 Future design

Following our conclusions from the previous section, we decided to take a step back and study the gate design employed by Zhang et al. [29] (Figure 12). Our goal was to first reproduce the results from the simulations in that work, before studying possible modifications to their design that could be beneficial for the confinement of smaller quantum dots. The main differences with respect to our gate geometry are: (i) the number of electrodes (this new design uses 6 local gates as opposed to the 8 gates in our design) and (ii) the shape of the gate electrodes (the outer gates are wider and have an inner semi-circular shape, to ensure a better and more regular confinement of the double dot). The reduced number of gates in this design already greatly simplifies the electrical tuning of QDs in the electrostatic simulations owing to the reduced number of parameters.

As a starting point, we observed that this new geometry greatly simplifies the confinement of single and double QDs, presumably due to the reduced number of

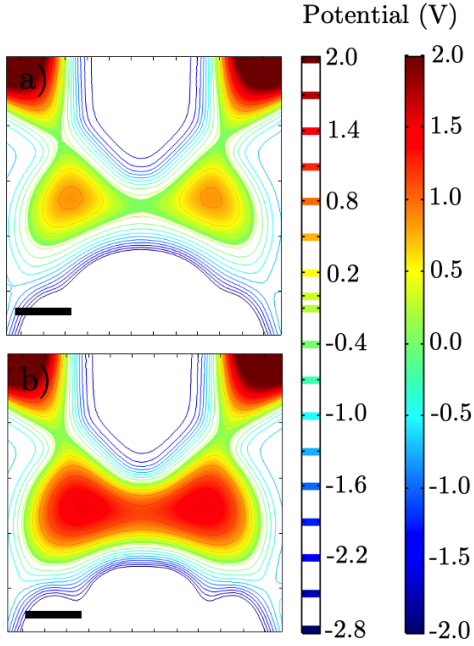


**Figure 22:** Simulation of the potential profile in the 5 nm MoS<sub>2</sub> layer for the electrode design of the device shown in Figure 12 as bottom gates for 5 nm of hBN with a scale bar of 50 nm. Here,  $V_{BG} = 15$  V,  $V_1 = -0.9$  V,  $V_2 = V_6 = -1.5$  V,  $V_3 = V_5 = -2$  V for both cases;  $V_4 = -3.2$  V (a) and  $V_4 = -0.8$  V (b). By tuning  $V_4$ , the transition between two single QD to a double QD can be observed.

gates and of cross-talk effects. Remarkably, we were able to electrostatically control the evolution of a single QD to a double QD, as shown in Figure 22, by tuning the central gates that control the interdot coupling.

The single QD shown in panel b) has an approximate dimension of 100 nm x 145 nm, whereas in the double dot configuration (panel a), each dot has a radius of approximately 60 nm. These results demonstrate that we are able to reproduce very well ref. [29], who reported a radius of  $\approx 68$  nm for the individual dots in a double QD configuration. While these values of QD dimensions seem encouraging, ref. [29] was unable to experimentally demonstrate the spin/valley character of confined charge carriers, which suggests that even smaller QDs are required (or experiments at a lower temperature are needed, in that work the measurements were taken at approx. 230 mK).

To evaluate the possibility of confining even smaller dots, we have slightly modified the above geometry (as shown in Figure 13) to reduce the overall dimension of the gate structure. Figure 23 reveals that this modification leads to a reduced radius of the individual dot in a double QD configuration (radius of approximately 40 nm), and therefore, would be beneficial towards demonstrating quantum dots with truly quantized energy spectra.



**Figure 23:** Simulation of the potential profile in the 5 nm  $\text{MoS}_2$  layer for the electrode design of the device shown in Figure 13 as bottom gates for 5 nm of hBN with a scale bar of 50 nm. Here,  $V_{BG} = 30$  V,  $V_1 = -2.8$  V,  $V_2 = -1.4$  V,  $V_3 = V_5 = -4$  V,  $V_6 = -1.5$  V for both cases;  $V_4 = -10$  V (a) and  $V_4 = -5$  V (b). By tuning  $V_4$ , the transition between two single QD to a double QD can be observed.

## 6 Conclusions

In this work, we take first steps towards fabricating devices based on few-layer TMDCs ( $\text{MoS}_2$  and  $\text{WSe}_2$ ) aimed at the confinement of single and double QDs and at the investigation of their fascinating underlying physics. This project is motivated by the prospects of studying the spin and valley textures of confined charge carriers in TMDCs, which has not been investigated at length by electron transport. Importantly, such a study could lead to possible applications in quantum technologies.

On the one hand, we have invested time towards developing the technology to fabricate devices based on 2D semiconductor TMDCs, including the exfoliation and stacking of van der Waals heterostructures, the optimization of the electrical contacts, the fabrication and optimization of local gates, etc. From this preliminary work, we have been able to advance on certain aspects of our devices, e.g., the isolation of the device channel from charged impurities in the substrate using hBN flakes, and the demonstration of working electrical contacts and local gates down to 4.2 K. While these developments are encouraging, some improvements are needed for obtaining devices with characteristics matching the state-of-the-art. To this end, we are currently exploring different methodologies to minimize the contact resistance, as

well as working on the implementation of graphite-based global gates.

Parallely, we have performed electrostatic simulations using the software COMSOL Multiphysics to evaluate the optimal device geometry for confining single and double quantum dots in few-layer TMDCs with reduced spatial dimensions. The main goal of this part of the thesis was to obtain guidelines for improving our device fabrication and thus, to maximize our chances to successfully realize the planned experiment. We observe that, while quantum dots with relatively large radius can be readily obtained, special attention is needed to reach the sub-100 nm regime needed for ensuring that the TMDC QDs display a quantized energy spectrum at reasonable temperatures. First, we have observed that the thickness of the hBN dielectric plays an important role. Indeed, by increasing the gate coupling with thinner hBN flakes, we were able to have a better control over the formation of local barriers and therefore over the confinement of QDs. In addition, we have observed that the arrangement of gate electrodes is crucial: too many gates in close proximity lead to cross-talk effects and thus to an overall reduced parameter space for the confinement of QDs. For the case of single QDs, we conclude that a simple geometry based on 4 local gates with a width of 35 nm is able to confine dots as small as 20 nm. On the other hand, for double quantum dots, our best results were obtained using a gate geometry slightly modified from that employed in ref. [29]. In this case, we were able to obtain dots with a radius of approximately 40 nm.



For the near future, we aim to implement the optimal gate geometries obtained in our electrostatic simulations already in the next generation of devices.

## 7 Acknowledgements

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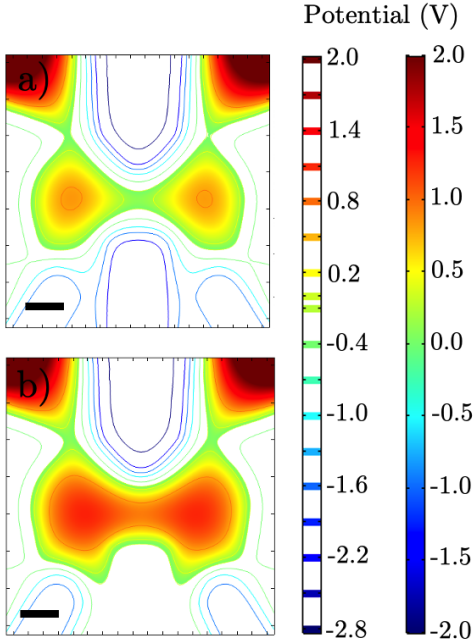
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## Appendices

### A WSe<sub>2</sub> simulations

As it was explained in the Simulations section, in our experiments, we also used WSe<sub>2</sub> as semiconductor due to its properties. For this reason, once we found a gates geometry that satisfies our requirements in terms of size, coupling and tunability of the QD, we tested it in a WSe<sub>2</sub>-based device (same configuration as Figure 12)

We simulated a structure with a 10 nm WSe<sub>2</sub> flake hBN bottom-encapsulated (5nm). In this device we could observe a large QD, tunable with the gates voltages (Figures 24). Indeed, this dot has similar size and shape as the one formed in the analogous MoS<sub>2</sub> structure and the values of the applied voltage for its control are also comparable. This result makes WSe<sub>2</sub> a suitable platform for studying these systems too. Indeed, there are no other double QDs simulations performed on this material in the literature.

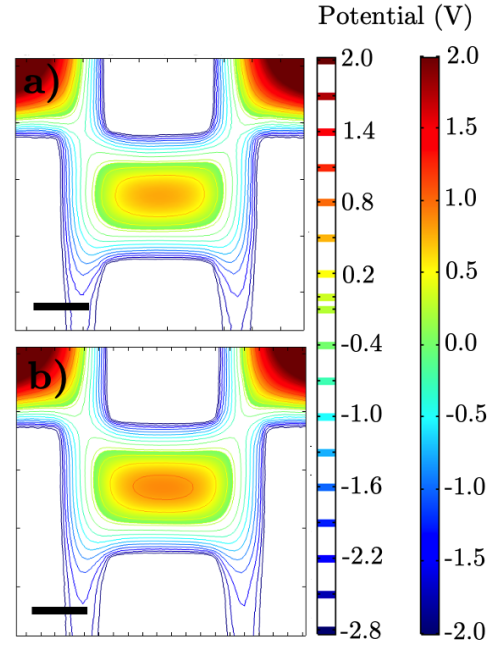


**Figure 24:** Simulation of the potential profile in the 10 nm WSe<sub>2</sub> layer for the electrode design of the device shown in Figure 12 as bottom gates for 5 nm of hBN with a scale bar of 50 nm. Here,  $V_{BG} = 15$  V,  $V_1 = -3$  V,  $V_2 = -0.5$  V,  $V_3 = V_5 = -2$  V,  $V_6 = -0.7$  V for both cases;  $V_4 = -0.25$  V (a) and  $V_4 = -2.6$  V (b). By tuning  $V_4$ , the transition between two single QD to a double QD can be observed.

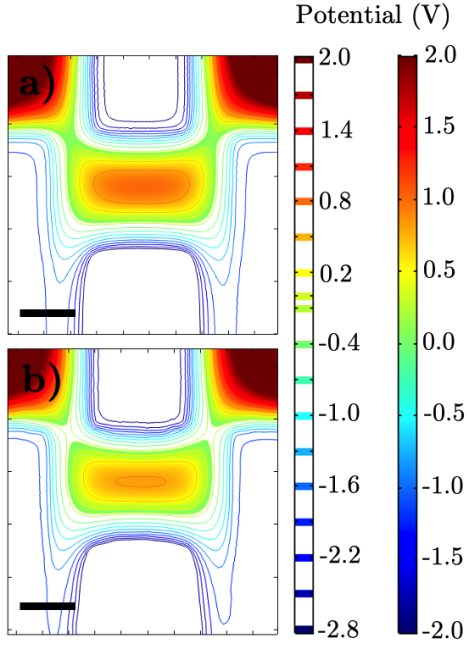
### B Encapsulated devices

As it was explained in the Sample fabrication section, charge impurities on the surface of the substrate can cause electrical switches in the behavior of the device. A way to avoid this effect is exfoliating a flake of hBN (dielectric) between the TMDC and the substrate. Hence, we also reproduced this configuration in our simulations as presented in Figure 25: the extra dielectric flake just causes slight differences with respect to the original structure (no changes in the coupling and small variations in the QD size) so, as an approximation, the simplified model without the second hBN flake, can be used for this computational study.

Moreover, in previous work, we shown that when having a bottom-gate configuration, if an hBN flake was exfoliated and transferred on the top of the semiconductor, the performance (contact resistance and field effect mobility) of the device considerably improved. Thus, we also simulated a fully-encapsulated configuration with bottom gates and compared it with the original configuration. The results can be seen in Figure 26: the extra dielectric flake slightly screens the effect of the back gate, leading to a potential profile equivalent to the original configuration with an extra 10 nm of hBN.



**Figure 25:** Comparison of the simulation of the potential profile in the 20 nm MoS<sub>2</sub> layer for same gate design as Figure 16. Device top-encapsulated (a) and fully-encapsulated (b) with a scale bar of 200 nm. Here,  $V_{BG} = 6$  V,  $V_1 = -3$  V,  $V_2 = V_4 = -2$  V and  $V_3 = -5$  V. Minor differences can be seen due to the effect of the bottom hBN flake on the voltage applied to the backgate.



**Figure 26:** Comparison of the simulation of the potential profile in the 20 nm MoS<sub>2</sub> layer for same gate design as Figure 17. Device bottom-encapsulated (a) and fully-encapsulated (b) with a scale bar of 200 nm. Here,  $V_{BG} = 6$  V,  $V_1 = -3$  V,  $V_2 = V_4 = -2$  V and  $V_3 = -5$  V. Minor differences between both are equivalent to an increase of 10 nm in the thickness of the hBN in the bottom-encapsulated device.

## C Simulations details

### Setting up the simulation

When using the physics interface Electrostatics in COMSOL, various default nodes are added to the Model Builder: Charge Conservation, Zero Charge and Initial Values. Then, other nodes can be implemented, such as boundary conditions and space charges.

Charge Conservation is the main node of this interface and adds the equation for charge conservation according to Gauss' law for the electric displacement field (Eq. 8). It provides an interface for defining the constitutive relation and its associated properties such as the relative permittivity  $\epsilon_r$  [22].

Initial Values adds an initial value for the electric potential  $V$  that can serve as an initial condition for a transient simulation or as an initial guess for a nonlinear solver [22].

The Zero Charge node adds the condition that there is no charge on the boundary so it satisfies Eq. 11. This is the default boundary condition at exterior boundaries. At interior boundaries, it means that no displacement field can penetrate the boundary and that the electric potential is discontinuous across the boundary [22].

Furthermore, additional conditions can be added. For this work, the Electric Potential node was also used, which provides an electric potential  $V_0$  as the boundary condition  $V = V_0$ .

### Parameters and other relevant information

Regarding the Mesh, we used a different user-controlled mesh for each geometry, according to the needs of the simulations. These typically consist on 50,000 – 200,000 elements in total, depending especially on the thickness of the hBN and the MoS<sub>2</sub> and the size of the top gates.

The detailed workflow in COMSOL is the following: firstly, under the Global Definitions tab, all the necessary Parameters were set, namely the thickness of the SiO<sub>2</sub>, of a monolayer of hBN, MoS<sub>2</sub> and WSe<sub>2</sub> and the number of layers to be used of each material in the simulation. Secondly, we imported the GDS file corresponding to the gate design in the subnode Geometry. From this first element, we built the whole 3D geometry, similar to the real devices used in our experiments. Next, we define the relative permittivities of the materials:  $\epsilon_{SiO_2} = 4.2$  [3],  $\epsilon_{hBN} = 3$  [33],  $\epsilon_{MoS_2} = 8.3$  for thicknesses less than 8 nm [34] (i.e., for 7 layers of MoS<sub>2</sub>  $\approx 5$  nm [35],  $\epsilon_{MoS_2} = 10.5$  for larger thickness [34] (i.e., from 14 layers of MoS<sub>2</sub>  $\approx 10$  nm) and  $\epsilon_{WSe_2} = 7$  [36]. Then, we assign a material for each domain of the geometry. After that, on the Electrostatics subnode, we define the boundary conditions: several voltage Terminals (top and bottom gates) and a backgate. Finally, we set a range of voltages for each terminal and the built-in FEM solver in COMSOL is invoked to solve the PDE problem.

## D Finite Element Method (FEM)

COMSOL uses the FEM to numerically solve a PDE problem. The following explanation was extracted from ref. [19]. The FEM is associated with variational (Ritz), a functional has to be minimized, and residual (Galerkin) methods while both lead nearly to the same equations. Poisson's equation with given boundary values is known as the strong form of an elliptical boundary value problem. To derive a functional it is necessary to introduce the weak form. Every problem in COMSOL is converted to the weak form in order to be solved using the FEM. Consider a stationary PDE problem

$$-\Delta u = f \quad \text{in } \Omega \quad (12)$$

where  $\Omega$  is the domain in which the Poisson equation has to be solved. Let  $v$  be an arbitrary test function. Multiplying the PDE by  $v$  and integration and application of Green's law results in:

$$\int_{\Omega} f v dx = \int_{\Omega} -\Delta u v dx = \int_{\Omega} \nabla u \cdot \nabla v dx \quad (13)$$

for all test functions  $v$ . Using the following notation shows the association to the linear  $\Omega$  functional  $F$ :

$$F(v) := \int_{\Omega} f v dx, \quad a(u, v) := \int_{\Omega} \nabla u \cdot \nabla v dx \quad (14)$$

The weak form requires less regularity of  $u$  and the variation principle is more fundamental. Now we have to find the solution  $u \in H$  that fulfills  $a(u, v) = F(v)$  for every  $v \in H$  ( $H$  is a Hilbert space). The idea behind the FEM is to solve the variation problem in a finite dimensional sub-domain  $H_h \subset H$  because it is very difficult to find test functions that approximately represent the true solution over the entire domain.

This discretisation relies directly on the fundamental variational principle and not on the PDE problem. The small regions (for example a triangle in 2D or a tetrahedral in 3D) are the finite elements and the points defining them are called nodes (degrees of freedom) while the assembly of the elements is called mesh. As the solution often does not vary much in a small sub domain, polynomials are commonly used as test functions. The solutions in the sub domains have to fulfill continuity conditions with the next element at the nodes or edges. Because the sub-domains have a finite dimension, a (nodal) basis can be chosen, which leads to a system of  $m = \dim H_h$  equations and unknown variables. These can be solved for each element with respect to the given boundary conditions (e.g. Gauss algorithm). Solving each element gives the solution of the entire domain. With a finer mesh, the solution becomes more accurate but it increases the degrees of freedom and hence, the calculation time. The FEM allows the mesh to be adjusted to the model geometry which is necessary to acquire a good solution.