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Multi-terminal electronic transport in boron nitride encapsulated TiS_3 nanosheets

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We have studied electrical transport as a function of carrier density, temperature and bias in multi-terminal devices consisting of hexagonal boron nitride (h-BN) encapsulated titanium trisulfide (TiS_3) sheets. Through the encapsulation with h-BN, we observe metallic behavior and high electron mobilities. Below ~ 60 K an increase in the resistance, and non-linear transport with plateau-like features in the differential resistance are present, in line with the expected charge density wave (CDW) formation. Importantly, the critical temperature and the threshold field of the CDW phase can be controlled through the back-gate.

Titanium trisulfide (TiS_3) is a van der Waals semiconductor with a direct band gap of ~ 1 eV. It has a crystal structure with Ti-S bond lengths longer in the b -direction than in the a -direction, forming two-dimensional (2D) sheets that are usually elongated along the b -axis. The one-dimensional chain-like lattice of TiS_3 is responsible for the large optical and electronic in-plane anisotropy [1, 2]. The anisotropic features along with the high mobilities and photo-response have established TiS_3 as a promising candidate for transistors [3–5] and polarization sensitive photodetectors [6, 7]. Furthermore, theoretical studies have suggested that monolayer TiS_3 has very high charge mobilities at low temperatures [8], rendering this material promising for studying quantum transport phenomena.

The electrical properties of bulk TiS_3 whiskers have been studied by Finkman *et al.* [9] and later on by Gorlova *et al.* [10, 11] who showed that TiS_3 exhibits semiconducting behavior (resistance increases with decreasing temperature) and below certain temperatures (57 K and 17 K) it undergoes a transition to a charge-density-wave (CDW) state due to a Peierls instability. Charge-density-wave transitions have also been found for other members of the family of the transition metal trichalcogenides (TMTCs) like NbSe_3 [12] and ZrTe_3 [13]. Very recently, the electrical properties at different temperatures of field-effects devices from TiS_3 nanoribbons were studied [14, 15]. Similar to other 2D semiconducting systems like MoS_2 [16] and WSe_2 [17] on SiO_2 , the devices showed disorder-induced electron localization even at high temperatures and high carrier densities. Moreover, degradation of the TiS_3 sheets during device fabrication procedure should not be excluded as a result of

polymer-impurity contamination, as well as to exposure to air and moisture even at moderate temperatures, similar to NbS_3 and MoS_2 [18, 19].

In this work we present results on electrical transport on multi-terminal TiS_3 field-effect devices. Via encapsulation with hexagonal boron nitride (h-BN), we minimize extrinsic sources of disorder and measure the intrinsic properties of this material. We study the conductivity (sheet resistance), the mobility and the current-voltage relationship as a function of temperature and electron density.

The boron nitride encapsulated TiS_3 heterostructures were fabricated using the van der Waals pick-up technique with polypropylene carbonate (PPC) films [20]. Prior to the stacking process, the top h-BN was pre-etched using a rich-in- CHF_3 gas reactive ion etching (RIE) process in order to deposit top metallic contacts (for more details see *Methods* section in the supplemental material) [21, 22]. Using the van der Waals based pick-up stacking of the heterostructures, the channel remains protected during the device fabrication procedure. Due to the narrow width of the sheets, the flakes were aligned so that the Hall bars have the long edge (b -axis) parallel to the voltage biasing direction, which is also the direction of the high conductivity [1]. The final stacks were deposited on Si/SiO_2 substrates, where the carrier density can be tuned by the Si back-gate. A schematic of the device cross-section is shown in Fig. 1a. Two devices of thickness 26 and 9 nm were fabricated, labeled as D1 and D2, respectively. In the main text we focus on results from sample D1 (inset of Fig. 1(c)). Similar results on the conductivity and mobility were obtained from sample D2 and can be found in the supplemental

material.

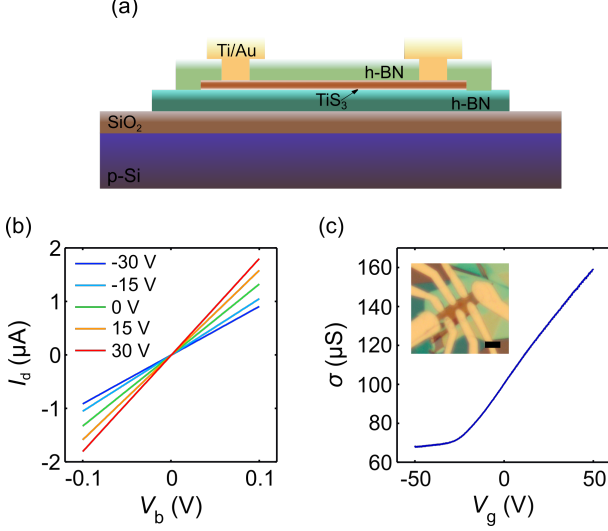


FIG. 1. Device schematic and room-temperature electrical characteristics. (a) Schematic illustration of the device cross-section consisting of a TiS_3 sheet encapsulated with h-BN. The Ti/Au contacts were deposited on TiS_3 through prepatterned windows in the top h-BN layer. (b) Current-voltage characteristics from two-terminal measurements for different back-gate voltages indicated in the legend. (c) Conductivity from four-terminal measurements as a function of the back-gate voltage. Inset shows the device that was used for the measurements (sample D1). Black scale bar corresponds to 3 μm .

Room-temperature electrical characterization in a two-terminal configuration verified the ohmic contacts from the drain current-voltage bias ($I_d - V_b$) characteristics at different back-gate voltages (V_g) (Fig. 1b). Using four-terminal measurements we obtain the intrinsic conductivity as a function of the back-gate voltage (Fig. 1c). We find an n -type semiconducting behavior similar to earlier reports [1, 4, 15]. The ON/OFF ratio appears to be small ~ 2.3 , while the threshold voltage is about -30 V from the onset of conductivity, indicating that large residual doping is responsible for the large current in the OFF state, in agreement with previous studies [4]. The room-temperature field-effect mobility, was calculated based on the relationship $\mu_{\text{FE}} = d\sigma / (C_g^{\text{FE}} dV_g)$, where $C_g^{\text{FE}} = 1.2 \times 10^{-4} \text{ F/m}^2$ is the gate capacitance determined by the parallel plate capacitor model and σ is the 2D or sheet conductivity. The mobility is found to be equal to 54 and $122 \text{ cm}^2/\text{Vs}$ for two- and four-terminal measurements, respectively. These mobilities are the largest reported so far for TiS_3 [3, 4, 15].

In order to investigate the conducting mechanism in the devices, we measured the conductivity as a function of back-gate and temperature using multi-terminal DC measurements at finite current bias (Fig. 2a). At all back-gate voltages, a decrease of the sheet resistance with

the decrease of the temperature is observed, which is a signature of metallic behavior. Nevertheless, below certain temperatures (which range between 70 and 150 K, depending on the charge carrier density) the sheet resistance starts to increase, which is a signature of insulating behavior (Fig. 2b). For negative gate voltages this up-turn takes place at high temperatures around 150 K. This behavior can be explained by a Fermi level alignment below the conduction band or mobility edge; when the temperature decreases the thermally excited carriers freeze out. For zero and positive gate voltage values we observe a metal-to-insulator-transition (MIT) at lower temperatures, but the resistance increase is more abrupt at higher gate voltages. This can be attributed to a CDW transition as expected at this temperature range for TiS_3 [10, 11]. The transfer curves in Fig. 2c, show that the conductivity increases with the decrease of the temperature down to 67 K for positive gate voltages. The threshold voltage defined as the back-gate voltage at which the conductivity starts to increase, shows a strong temperature dependence as a consequence of the aforementioned carrier freeze-out. Below 67 K the conductivity starts to drop and as the temperature decreases, the transfer characteristics show a sublinear ‘bending’, indicating enhancement of the insulating state at higher electron densities (Fig. 2d).

In semiconductors and metals one of the most important figures of merit is the carrier mobility, and to calculate it from the conductivity based on the Drude model, the carrier density should be known. To obtain the carrier density, we performed Hall measurements at various temperatures (75, 90, 150, 250 K). Figure 3a shows the carrier density, which increases in a linear way with the back-gate voltage; it equals $6\text{--}12 \times 10^{12} \text{ cm}^{-2}$ for $V_g = 0\text{--}50$ V. From this measurement we obtain a capacitance per unit area of $1.9 \times 10^{-4} \text{ F/m}^2$, which is larger than the estimated one from the parallel plate capacitor model ($1.2 \times 10^{-4} \text{ F/m}^2$, for $\epsilon_{\text{hBN}} = 4$). Based on the Drude formula $\sigma = n_H e \mu_H$, where e the electron charge, n_H the electron Hall density and μ_H the Hall mobility, we calculate the Hall mobility as a function of the back-gate voltage. At 90 K, μ_H is found to be between 250 and $330 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ for $V_g = 0 - 50$ V (Fig. 3a). This result demonstrates that the device exhibits high electron mobilities due to the encapsulation with h-BN, although the mobilities are lower than those of TMDCs and black phosphorus when using similar encapsulation techniques [23–25]. Also, the large residual density for $V_g = 0$ V, shows that the TiS_3 sheet contains a large density of impurities that probably originates from sulfur vacancies as in the case of the TMDCs [26–28], thereby limiting the mobility in the device.

The mobility usually depends on the temperature with a power law: $\mu \propto T^\gamma$. The value of the coefficient γ can reveal the dominant scattering mechanism of the electrons. A γ in the range of -0.5 and below, is a signature

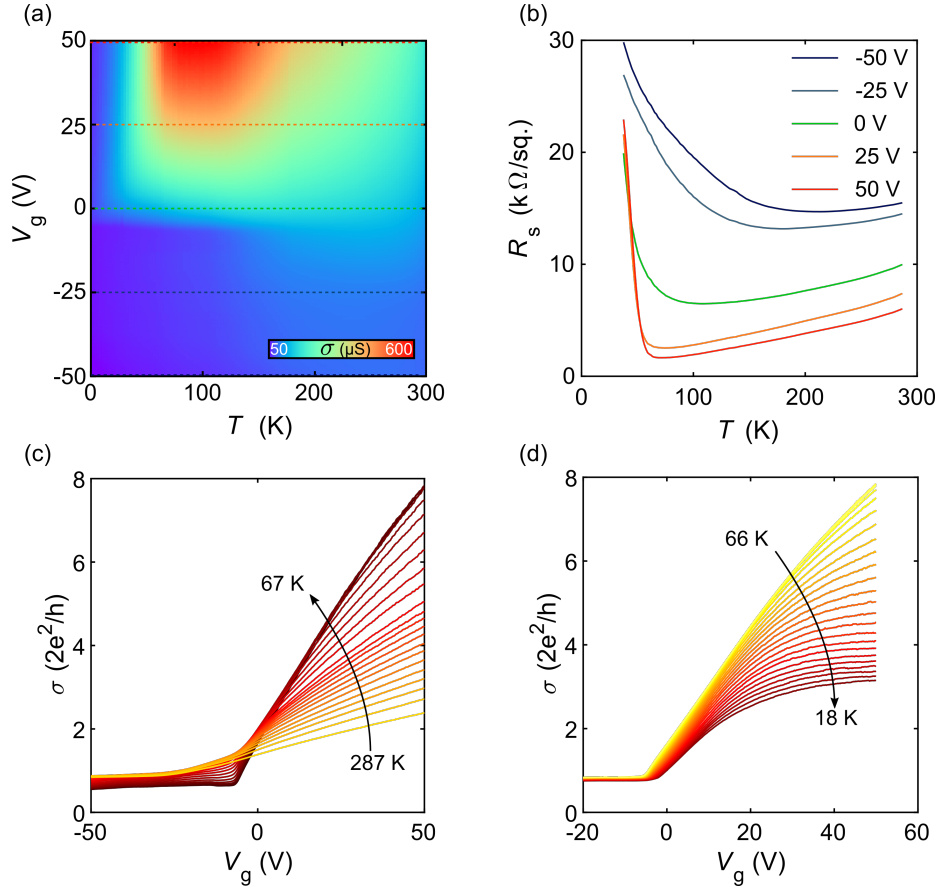


FIG. 2. Temperature and gate dependence of the conductivity/sheet resistance. (a) Colormap of the conductivity as a function of temperature and back-gate voltage. The horizontal dashed lines correspond to the temperature traces at constant gate voltages of the sheet resistance plotted in panel (b). (b) R_s vs. T for different back-gate voltages. Conductivity vs. gate voltage characteristics for temperatures between 67 and 287 K in (c) and between 18 and 66 K in (d). The datasets of panels (a), (b) and (c) were obtained using $I = 100$ nA, while the dataset in panel (d) was obtained with $I = 20$ μA .

of phonon scattering [29]. At very low temperatures, γ can approach 0 (mobility independent from temperature), which is the case of impurity scattering for degenerate semiconductors, while in non-degenerate semiconductors with substitution doping $\gamma = 3/2$ [30, 31]. In Fig. 3b, we plot on a logarithmic scale the field-effect and the Hall mobilities (for $n_H = 9 \times 10^{12} \text{ cm}^{-2}$) as a function of the temperature from 200 to 75 K. The Hall mobility was calculated using the Drude formula as mentioned above, while the field-effect mobility was obtained from the transconductance through the relationship $\mu_{\text{FE}} = \delta\sigma / (C_g^{\text{FE}} \delta V_g)$, with a linear fit in the σ - V_g plots of Fig. 2c around $V_g = 0$ V. As found usually, the Hall mobility is 2-3 times smaller than the calculated field-effect mobility [17, 25]. From the linear fit of the data in this $\log_{10}(\mu)$ vs. $\log_{10}(T)$ plot, we obtain the coefficient γ in the temperature range of 75 to 280 K. The value of γ is -1.2 and -2.0 for the Hall and field-effect mobilities, respectively, indicating phonon scattering in this temperature range [29]. We attribute the discrepancy

between the two γ values to the Hall scattering factor (r_H) that can be different than unity [32, 33] and is defined as $r_H = \mu_H / \mu_{\text{eff}}$ where μ_{eff} is the effective or drift mobility, or equivalently $r_H = C_g^{\text{FE}} / C_g^{\text{H}}$, with C_g^{H} the capacitance per unit area based on Hall measurements. Since the capacitance of the gate dielectrics is not changing with temperature, the temperature dependent gate capacitance from Hall measurements (Fig. S7) indicates a non constant Hall scattering factor. The Hall scattering factor in this case is found to be equal to 1.3 at 200 K and decreases to 0.4 at 75 K.

Metal-insulator transitions (MIT) or charge density wave (CDW) transitions are usually associated with non-linear transport with distinct characteristics. In the case of CDW, the lattice rearranges due to a Peierls instability and an electronic gap opens at the Fermi level due to the formation of the standing electron wave [34]. Pinning of the CDW to impurities leads to bias dependent transport. In the differential resistance a plateau appears around zero bias and above a critical field depinning leads

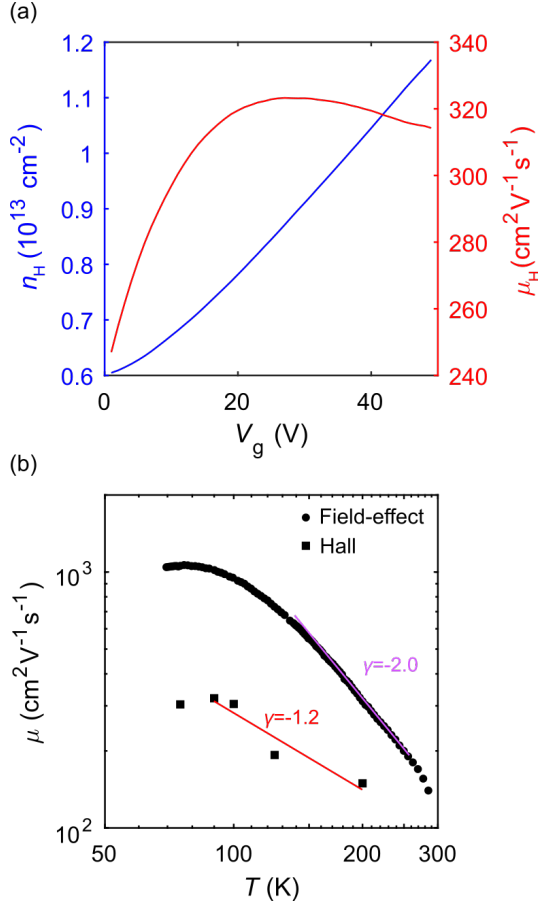


FIG. 3. Mobility of device D1. (a) Electron density (blue solid line) from Hall measurements and Hall mobility (red solid line) as a function of back-gate voltage at $T = 90 \text{ K}$. (b) Logarithmic plot of the field-effect (circles) and Hall mobilities (at $n_H = 9 \times 10^{12} \text{ cm}^{-2}$) (squares) as a function of the temperature. At high temperatures the dependence is approximately linear following a power law dependence ($\mu \propto T^\gamma$). For the field-effect mobility $\gamma = -2.0$, while for the Hall mobility $\gamma = -0.9$.

to an abrupt decrease of the differential resistance. MITs, on the other hand, originate from carrier localization due to strong disorder. In this case hopping of electrons is strongly temperature and electric field dependent albeit without an abrupt change with electric field [35].

Figure 4a presents voltage-current bias (V_p - I) curves for $V_g = 50 \text{ V}$ from four-terminal measurements that show almost linear behavior for high temperatures, but below 66 K they become strongly non-linear. In the differential resistance a strong peak at low current bias is evident, which forms a plateau upon lowering the temperature (Fig. 4b). Figure 4c shows I - V_p characteristics for different gate voltages at $T = 4 \text{ K}$. The shape of the V_p - I curves shows clear signatures of a CDW phase as in the case of NbSe_3 [36, 37]. From the differential resistance the critical (or threshold) electric-field of the sliding

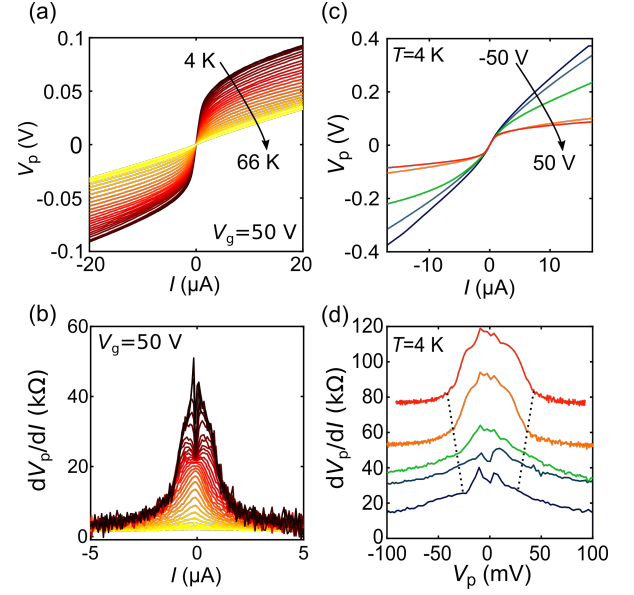


FIG. 4. Low-temperature non-linear transport properties. Probe-voltage (a) and differential resistance (dV_p/dI) (b) as a function of the current bias for different temperatures below 67 K for $V_g = 50 \text{ V}$. (c) V_p - I characteristics for different gate voltages at $T = 4 \text{ K}$. (d) Differential resistance as a function of the probe-voltage for the same gate voltages and temperature as in (c). The curves have been shifted vertically for clarity. Dashed lines indicate the critical voltage (E -field) of the sliding CDW.

CDW estimated to be 120 V/cm for $V_g = 50 \text{ V}$, where the transition can be seen more clearly (Fig. 4d). For lower gate voltages the I - V_p characteristics indicate a reduction of the critical field but as the curves are more smeared, it is difficult to extract accurate values.

Since the non-linear current-voltage curves indicate a CDW phase, we will follow with an analysis that is usually carried out to investigate the critical temperature of the CDW transition. The zero-bias differential resistance (R_{s0}) as a function of T for three different gate voltages is plotted in Fig. 5a. A cusp is present at temperatures of $\sim 60 \text{ K}$, followed by an increase in the resistance and a second cusp just below 20 K indicating the presence of two transitions. Such anomalies in the differential resistance are evidence for a CDW transition due to the formation of the gap and have been observed in different materials [38, 39]. For higher bias, the CDW features vanish (Fig. S6) [12]. Plotting the logarithmic derivative $d(\ln R_{s0})/d(1/T)$ vs. T , the CDW transition temperature can be determined from the maximum of the curves (Fig. 5b). There is a clear peak-like shape curve with a maximum around 60 K and zooming-in around 20 K there is a small bump visible (inset of Fig. 5b). Figure 5c presents the dependence of the temperatures of the two transitions on the back-gate voltage. The first transition exhibits an increase from 42 K to 52 K when the

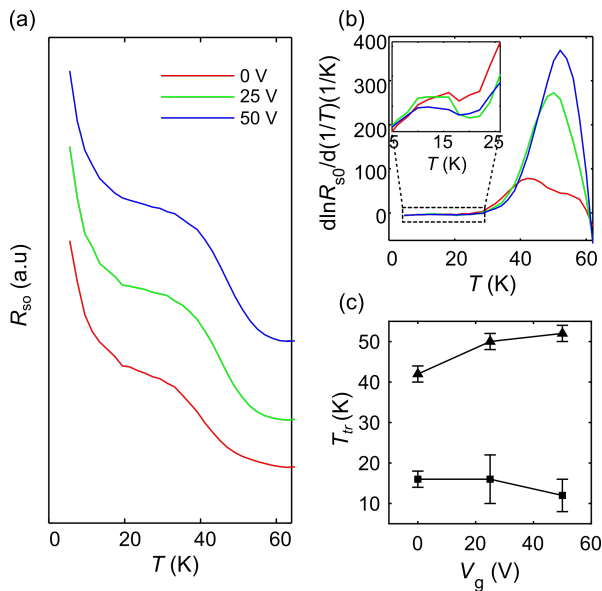


FIG. 5. CDW analysis of resistance versus temperature curves. (a) Temperature dependence of the zero-bias differential resistance (R_{s0}) for different gate voltages. The curves have been shifted vertically for clarity. (b) $d(\ln R_{s0})/d(1/T)$ vs. T . From the inflation point the critical temperatures associated with the CDW have been determined. The inset shows a zoom of the dashed area at the low temperature regime, where a second inflation is present. (c) Critical temperatures as a function of the gate voltage.

gate voltage increases from 0 to 50 V. In bulk samples and along the b -direction the critical temperature was found equal to be 59 K [11], close to the values obtained here. Such a modulation of the transition temperature was also found in NbSe_2 and TaS_2 recently [40]. On the other hand, the second transition, which is found around 16 K for $V_g = 0$ V shows a weak gate dependence and drops to 12 K at $V_g = 50$ V. Since the uncertainty of this critical temperature is large, we cannot determine with certainty whether it increases or decreases with the back-gate voltage.

Sample D2 also shows signatures of a CDW at high carrier densities (see Supp. Info for the analysis). At $T = 4$ K the differential resistance at for instance $V_g = 80$ V shows a clear plateau with a critical electric field of 112 V/cm, in agreement with that of sample D1 (Fig. S4a). Following the same analysis as done with sample D1, we find the maximum of the curve in the $d(\ln R_{s0})/d(1/T)$ vs. T plot in the range of 50-56 K, a value again close to the value for sample D1. At low carrier densities, i.e., at low gate voltages, the behavior for sample D2 differs from that of sample D1. For example at zero gate voltage, the differential resistance does not show a plateau but instead a peak around zero bias (see Fig. S4a). Such a behavior indicates the presence of a MIT rather than a CDW. With increasing gate voltage ($V_g > 20$ V) the

plateau-like feature in the differential resistance starts to develop with the zero-bias peak superimposed on it. As the gate voltage increases, the zero-bias peak decreases in amplitude and vanishes at the highest gate voltages as discussed above. At the same time for gate voltages larger than 20 V the maximum in the $d(\ln R_{s0})/d(1/T)$ remains close to the 50-52 K value found for high gate voltages. Apparently, charge localization and the formation of a CDW phase compete in this range of gate voltages. It is interesting to note that in this transition region, the CDW transition temperature of 50 K and the critical field are consistent with the values found in the thicker sample D1.

In summary, we have studied electrical transport in exfoliated TiS_3 encapsulated in boron nitride. The mobilities of our samples are the largest reported for this material, highlighting the encapsulation with boron nitride as a useful approach to improve sample quality. Moreover, we found that the thicker sheet shows clear evidence for a CDW transition, while the thinner shows CDW features along with an overlapping MIT. The T_{CDW} of the two samples is in agreement with reports in bulk samples [11] as well as with indirect evidence in nanoribbons [15]. Our results provide clear evidence that quantum phase transitions can be controlled in TiS_3 rendering the particular system interesting to study many-body physics.

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