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Sub-harmonic oscillations attenuation in hardware-in-the-loop models using the Integration Oversampling Method

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ABSTRACT

Hardware-in-the-loop (HIL) technology has become widespread for testing purposes, gaining special importance in micro-grids and renewable energy. One of the main challenges in HIL technology is its use in mid or high-frequency applications. In those cases, oversampling gate signals is a must to obtain enough accuracy and avoid undesirable sub-harmonic oscillations in the emulation that would not appear in a real scenario or offline electrical simulation. However, handling the extra information obtained through oversampling increases significantly the complexity of switched models since the oversampling methods deal with more than one sample per simulation step. It leads to extra design effort if the models are designed ad-hoc or increased hardware resources when using vendor tools that implement oversampling techniques. In both cases, oversampling traditionally implies an increase in the overall cost of the HIL system. This paper proposes the Integration Oversampling Method (IOM), which manages the extra information obtained through oversampling with a minimum impact on the models' complexity. In fact, the power model is not changed at all and uses just one switch state per simulation step. The method consists in adding a small hardware block in the input of the gate signals. Using the additional information obtained through oversampling, it generates a set of switch states in every simulation step that minimizes the integrated error in the input reading. The experimental results obtained through an NI myRIO device show clearly enhanced performance when using IOM both in transient and steady-state operation. At the same time, the additional hardware resources necessary for IOM implementation are negligible.

1. Introduction

Hardware-in-the-loop (HIL) is a real-time (RT) simulation technique that enables emulating the behavior of a part of a system to test the performance of the overall system both in ordinary and abnormal scenarios [1–3]. It can be used in multiple applications such as a low-voltage circuit breaker [1], doubly-fed induction generator control board [2], or modular multilevel converter based high voltage direct current [3]. HIL simulation becomes a vital part of power electronic controllers' development due to its lower risk, cost, prototyping effort, and build-up time [4]. The current trend in HIL tests is to achieve simulation results closer to the real systems using fewer hardware resources (lookup tables, flip-flops, and digital signal processing blocks) [5,6]. Ref. [5] provides a method to calculate the word length of the HIL model signals to optimize hardware resources and to reach high precision. The HIL model accuracy is also studied in [6].

Low latency is extremely demanded to maintain the HIL model fidelity [7,8]. The RT simulator proposed in [7] achieves a time-step of 1 μs regardless of the size of the application. The same time-step is achieved in [8] using a graphical user interface for designing the HIL model. In high-frequency HIL applications such as [9–11], which are prevalent by advances in wide-bandgap semiconductors' technologies, it is vital to reach short latencies. The smaller the latency, the smaller the HIL model error, as shown in [12]. Consequently, Field Programmable Gate Arrays (FPGAs), due to their parallel computing ability, have been used recently to reach accurate HIL models of power converters with a time-step around or below 1 μs [13,14]. For example, a simulation step (T_{ss}) of 680 ns is achieved in [13] using Vivado HLS as a design approach for the FPGA-based RT simulation of an NPC converter. The impact of other design approaches on the minimum achievable T_{ss} is studied in [15]. Nevertheless, the achievable time-steps in the HIL models are usually not accurate enough to sample the gate signals properly. For instance, 1 μs, as sampling time for a gate signal, may lead to significant errors and sub-harmonic oscillations that would not appear in real converters or offline simulators. Because if an

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intra-step switching transition occurs, the HIL models will apply it at the next T_{ss}, which causes discretization inaccuracy.

The sideband consequences caused by the input sampling process may threaten the validity of the HIL models or generally any RT simulators with a fixed time-step [16]. It is even more likely if the input sampling frequency is relatively close to the switching frequency. As reported in [17–20], the interaction between the controller and the power converter HIL model could cause instability issues such as low-frequency oscillations since the PWM transition may be in asynchronism with the HIL model time-step. A PWM voltage source converter-based D-STATCOM system is used as a case study in [17]. Ref. [18] uses a three-phase converter to address the problem. The numerical oscillations caused by the sampling process in electromagnetic transients simulation are reported in [19]. The same issue in a HIL model of a voltage source converter-based HVDC system is reported in [20]. A comprehensive analysis of these low-frequency oscillations in HIL systems, called aliasing distortion, is presented in [21] by using a boost converter HIL model as a case study. However, the solution for alleviating the unexpected aliasing distortion is not discussed in that paper.

The solution for this lack of resolution in the gate signal is oversampling. Therefore, more than one gate signal value is sampled every time-step of the model. This increases the complexity of the HIL models since circuits are not just ON or OFF during each time-step. Nevertheless, this is the solution that has been adopted in RT simulators recently. A review of several oversampling methods used in RT simulators is presented in [22]. It highlights that the common idea in all oversampling methods is to detect the switching transition moments precisely [23,24]. The extra achieved information by the input oversampling allows HIL models to compute the output more accurately without modifying the T_{ss}. Interpolation/extrapolation methods are one of the oversampling approaches that can be adopted in HIL systems [25]. They use the exact switched model of the converter. For instance, a switched model of a voltage source converter is used as a case study in [26] to validate the performance of the interpolation method in HIL applications. However, recalculating the state variables when switching events occur during simulation slows down the model, especially for recent power converters with a high number of switches [27]. The model accuracy can be significantly enhanced by interpolating the signals and estimating them in the transition moment. However, applying oversampling techniques to the HIL models increases the computation burden due to the model complexity, as cited in [25]. Thus, these methods have been rarely used in conventional HIL setups. The time average (sub-cycle averaging) method [28] is another oversampling approach that HIL systems can use. It reads the average values of the inputs for generating the next step values, but based on average state variable values. Therefore, there is no switching ripple, for instance. A detailed comparison between interpolation/extrapolation methods and the time average method is presented in [29]. It shows that the average model of the converter can easily support multiple switching events. However, as shown in [30], it cannot be applied to the switched model of converters.

Recently, Typhoon HIL exploited the oversampling method in their HIL products using the technique called Global Gate Drive Signal oversampling (GGDSO). Apart from the extra complexity of the GGDSO algorithm, it can only be applied to the HIL systems with only one switching transition within a single T_{ss} since it uses the interpolation method [31,32]. In contrast to GGDSO, another oversampling algorithm, called Switch-level GDS oversampling (SGDSO), is presented by [32] to overcome this challenge. It calculates the model's output based on the average value of the input sampled with oversampling step (T_{is}) that has a higher frequency than the T_{ss}. However, SGDSO demands further hardware resources in comparison with GGDSO. It is recommended by [33] not to use the SGDSO method for switched converters operating in switching frequencies below 4 kHz.

This paper presents a new oversampling method called Integration Oversampling Method (IOM) to attenuate the aliasing distortion seen in HIL systems. The HIL model using IOM does not need to be changed because it will still use one single gate signal status (ON or OFF) during each time-step. However, the additional information obtained through oversampling is used to decrease the overall error produced by time-steps that are not completely ON or OFF steps. IOM is generated in an external block to the power converter model, between the real gate signal input and the model gate input. The input oversampled information is analyzed only in the IOM block, independently of the converter model, and it decides whether to apply ON or OFF status to the switched model of the converter when a mixed ON/OFF time-step is detected. Thus, IOM does not modify the HIL model T_{ss} unlike the other oversampling methods that involve the input oversampled information in the switched model. This paper investigates the applicability of the proposed method to the HIL model of power converters working on mid/high frequencies. The input sampling error and the distortion in the frequency domain are analyzed by using an ideal boost converter. The analysis shows that the proposed method can eliminate high-amplitude output steady-state fluctuations both in open-loop and closed-loop.

Following this introduction, the switched model of a boost converter and its equations are introduced in Section 2. Section 3 describes the aliasing issue found in HIL models using the boost converter as an application example. Section 4 presents IOM as a technique that reads the input with a higher effective resolution to attenuate the aliasing distortion explained in Section 3. It allows using longer T_{ss} even for high-frequency applications. Offline MATLAB simulation results and experimental results obtained by implementing the HIL model using IOM in an NI myRIO setup are given in Section 5. A comprehensive comparison is illustrated in this section by comparing simulations and NI myRIO experimental results enabling/disabling IOM. Finally, the conclusions which sum up the salient contributions of IOM are given in Section 6.

2. Application example

This section introduces the application example used as a case study throughout this paper. In particular, it will provide the equations of an ideal boost converter needed for implementing its HIL switched model in an FPGA with a fixed discrete T_{ss}. It is important to notice that a very simple example has been chosen as the case study in order to focus on the proposed IOM technique, not the details of the switched HIL model. In [21] it was shown that the effects of inaccurate sampling of the input gate signals, such as sub-harmonics, appear independently of the complexity of the model. For instance, sub-harmonics appear regardless of whether the model includes losses or not. For the sake of clarity, a simple topology has been chosen since the objective of this paper is not to show which HIL models are more accurate but to show the effects of adding the IOM technique to any switched HIL model that uses a single switch state per simulation step. In that way, the HIL model, which is not the paper's objective, can be presented and understood easily, focusing on the proposed IOM technique.

For the presented HIL switched model of a boost converter, all equations are discretized by using an explicit Euler ODE solver for the sake of simplicity and minimum hardware consumption. Boost converters are prevalent in many industrial applications, and they are also among the HIL applications that demand high resolution (small T_{ss}) due to their high switching frequency. So, an ideal boost converter shown in Fig. 1 is used in this paper. Anyhow, the main conclusions are valid for any other switching converter topology, with or without losses [21]. The input voltage is denoted by V_{in}, and the values of the inductor (L) and the capacitor (C) can be chosen based on the switching frequency and power ratio. The specific values used for the case study are shown in Table 1.

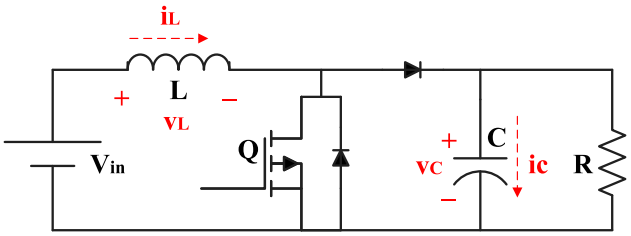

Fig. 1. Ideal DC/DC boost topology.

The HIL model implemented in FPGA computes the state variables (the inductor current (i_L) and the capacitor voltage (v_C)) from the previous values by adding the incremental values to them each time step. State variables of the boost converter are defined by the evolution of the capacitor voltage and inductor current, as seen in (1) and (2).

$$v_C(k) = v_C(k-1) + \frac{\Delta t}{C} \cdot i_C(k-1) \tag{1}$$

$$i_L(k) = i_L(k-1) + \frac{\Delta t}{L} \cdot v_L(k-1) \tag{2}$$

where i_C (the capacitor current) and v_L (the voltage across the inductor) corresponding to the possible switching states are given by (3) and (4). The step of the state variables is denoted by k, and Δt is the same as T_{ss}. In RT simulations, Δt must be greater than the time needed for the execution of the model equations.

$$i_C = \begin{cases} -\frac{V_C}{R} & Q : on \\ i_L - \frac{V_C}{R} & Q : off \end{cases} \tag{3}$$

$$v_L = \begin{cases} V_{in} & Q : on \\ V_{in} - v_C & Q : off \ \& \ i_L > 0 \\ 0 & Q : off \ \& \ i_L \leq 0 \end{cases} \tag{4}$$

The schematic of the switched model of the ideal boost converter implemented based on the equations presented in this section is shown in Fig. 2. This model implemented in an FPGA will be kept unchanged using IOM. In contrast, the model must be modified using other oversampling methods. For instance, the sub-cycle average method cannot be applied to the switched model of the converter. It reads the average values of switches within a T_{ss} by oversampling the input signals. Then it applies them to the average model of the converter, a model totally different from the switched model. The interpolation method, extrapolation method, or a combination of them can be applied to the switched model of power converters. However, they increase the complexity of the system (especially if multiple switching events occur in a single T_{ss}) because the model must be able to recalculate the accurate values of all signals at detected transition moments by the oversampling resolution. Therefore, IOM is the only proposal that allows using oversampling in switched models without changing the model, i.e. using a single switch state in the model per simulation step.

3. Aliasing distortion in HIL models

The gate drive signals' transitions are rarely synchronized with the HIL model T_{ss}, which results in output distortion. The problem arises when the input sampled signal precision is insufficient to allow the HIL model to produce the output with the desired accuracy. It can be even more critical when the sampling and switching frequencies are such that aliasing produces low sub-harmonic oscillations since power converters do not naturally filter low frequencies. These low-frequency oscillations can be the primary source of error in power converter HIL models that confuse the appropriate behavior of the controller.

Table 1
The simulation parameters of the boost converter.

Parameters	Values
Input voltage	$V_{in} = 12$ V
Inductor	$L = 800$ μH
Capacitor	$C = 80$ μF
Output voltage	$v_o \approx 20$ V
Load	$R_o = 12$ Ω
Output power	$P_o = 34$ W
Simulation step	$T_{ss} = 500$ ns
Duty cycle	$D = 0.42$
Switching period	$T_{sw1} = 9899.93$ ns $T_{sw2} = 9999.947$ ns

The aliasing frequencies ($f_{aliasing}$) can be formulated as (5) where T_{is} and T_{sw} are the input sampling period and the switching period, respectively and LCM stands for the least common multiple. In many HIL applications, T_{is} equals to the simulation step (T_{ss}), although the maximum input sampling frequency can be drastically higher than the simulation step frequency. For example, the digital inputs in Typhoon HIL402 device have a resolution of 30 ns while its T_{ss} is 1 μs [34]. Decreasing T_{is} attenuates the aliasing oscillations for two main reasons. First, it shifts the aliasing frequencies to the range over the switching frequency of power converters. These sub-harmonics will be filtered by the converter. Second, reading the input signal with a higher resolution will reduce the sub-harmonics amplitude due to the sampling error reduction.

$$f_{aliasing} = \frac{n}{LCM(T_{sw}, T_{is})}, \qquad for\ n = 1, 2, 3, \ldots \tag{5}$$

Fig. 3 shows the sampling effects for a boost converter HIL model obtained by MATLAB simulation. The reference waveform (shown in blue) is the simulation of a boost converter with a T_{ss} of 1 ns to avoid discrepancies caused by sampling. The simulation parameters are presented in Table 1. The switching periods of 9900 ns or 10 000 ns are selected since the oscillations will be totally different when T_{sw} is a multiple or non-multiple of T_{ss}. As can be seen in Fig. 3, the oscillations period will be shorter for non-multiple cases than for multiple ones. In fact, there would be only offset error without oscillations when T_{sw} is a perfect multiple of T_{ss}, as reported in [21]. However, it is almost impossible to reach those ideal T_{sw} values in experimental tests since the real T_{sw} must be a multiple of the controller's master clock, which is also not ideal. Therefore, the final T_{sw} (9899.93 ns and 9999.947 ns) are chosen based on the exact values obtained by the experimental tests to reproduce the same pattern via simulation reaching a close agreement with the experimental results, as will be shown in Section 5.

As illustrated in Fig. 3, by modifying the T_{sw}, the model will read different periods of the D resulting in different oscillations. A longer period of the D when the T_{sw} is closer to a multiple of T_{ss} creates more significant oscillations in the inductor current. For instance, in Fig. 3(b), the HIL model reads a bigger value of D (0.45) for 3810 switching periods and then a smaller value (0.40) for 5714 switching periods. In this example, the original D is 0.42, and the maximum possible D error could be up to 0.05 obtained by (6). It reveals that the D read by the HIL model has the same average value as the original PWM

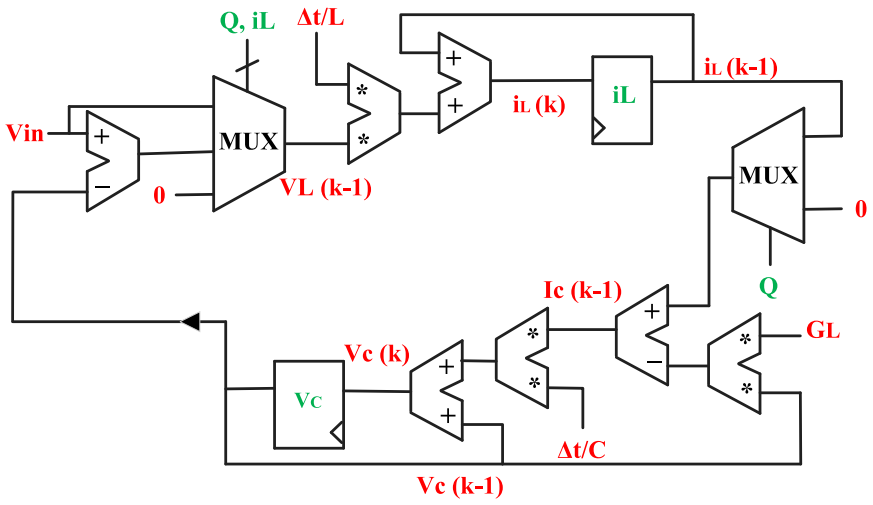

Fig. 2. Digital model of the ideal boost converter.

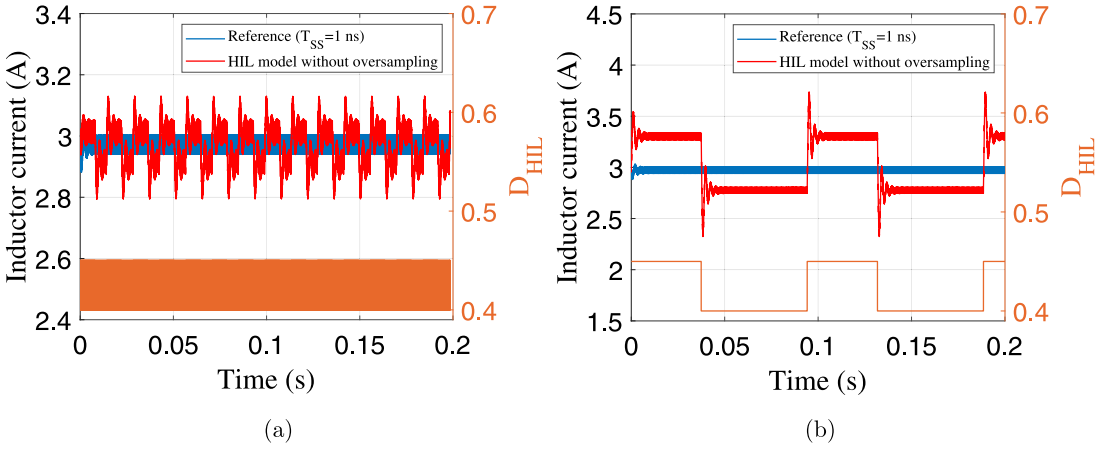

Fig. 3. The inductor current distorted by the aliasing issue in the HIL model of a boost converter when $T_{ss} = 500$ ns (shown in red) comparing with the reference current (shown in blue), and the duty cycle pattern read by the HIL model (displayed in orange); (a) $T_{sw} = 9899.93$ ns, (b) $T_{sw} = 9999.947$ ns.

but includes low-frequency variations, distorting the results. These sub-harmonics can create even bigger oscillations if they are near the resonant frequency of the model.

$$e_{D,max} = \frac{T_{ss}}{T_{sw}} \tag{6}$$

The aliasing distortion propagates throughout the HIL model causing more problems in the rest of the system. Due to the tendency to use HIL in high-frequency applications, the commercial T_{ss} resolution is insufficient for the input sampling process. Thus, oversampling methods are crucial to eliminate the aliasing distortion in new HIL systems. The main contribution of this paper is to break the long periodic pattern of the input by using a proposed oversampling technique called IOM. It can minimize the HIL model inaccuracies, including aliasing oscillations and offset error, which have been introduced in this section.

4. Integration oversampling method

IOM is a method for decreasing the error of HIL models due to inaccurate duty cycle reading. The method is based on oversampling the gate signal. However, it uses an independent block (IOM) to handle this additional information instead of changing the HIL model. It allows using the same HIL model (switched model) with one single input sample per simulation step. The method considers the error on the input between the oversampled input and the effective gate signal driven to the model, which is just one single ON or OFF value for every simulation step. Of course, there is error only during gate transitions, when the gate signal is not just ON or OFF during a whole simulation step. This error is integrated (i.e., accumulated), taking it into account for changing the following gate values that will be sent to the power converter model, in a similar way to the principle of sigma-delta modulators. Thus, IOM embedded inside HIL models can be employed as an effective way to improve accuracy by modifying the read input signal pattern. It avoids low sub-harmonic oscillations that produce big errors, while the model is not internally modified. The block diagram of the HIL model using IOM is composed of the switched HIL model block and the isolated IOM interface block connected before the HIL model, as depicted in Fig. 4.

IOM accumulates the fractions of ON time until a complete T_{ss} is integrated, and then it applies the accumulated ON time to the HIL model. The time resolution for reading the input is T_{is}, so there will be $N_{os} = T_{ss}/T_{is}$ fractions in each simulation step. IOM algorithm is explained as a flowchart in Fig. 5. In this flowchart, IOM reads the input signal, and the output signal is generated as an input for the HIL model. The number of fractions (F) is incremented by 1 every time the gate signal is ON ($Input = 1$) in a rising edge of the T_{is} clock. The F counter clock is synchronized with the input sampling frequency, and it stops counting and holds its value when the input is at a low level ($Input = 0$). When the number of fractions reaches N_{os}, the integer (I) is increased in the form of a carry bit, and F starts over at 0 where the

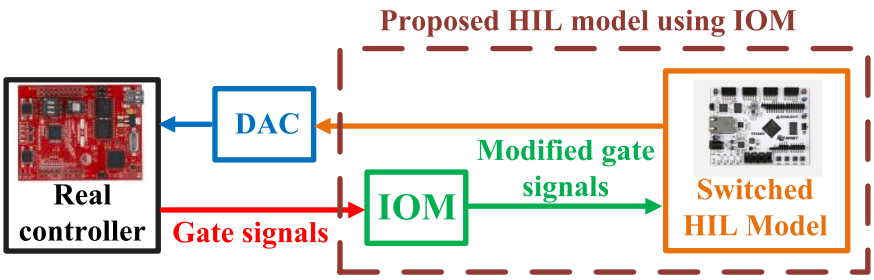

Fig. 4. Basic elements of a general HIL system based on IOM.

previous F is $N_{os}-1$ and the input is at a high level (F counts up from zero to $N_{os}-1$). This is equivalent to measuring the gate signal at a high level for a complete simulation step. The auxiliary 1-bit I signal, generated in the IOM, contains all the extra information obtained by the input oversampling. Whenever $I = 1$, the method waits until the next T_{ss} rising edge and then applies a complete ON T_{ss} cycle to the model. At this moment, I is reset from 1 to 0 since the integrated T_{ss} period has already been applied. Then, I will wait again for F overflow (changing from $N_{os}-1$ to 0), meaning that a new T_{ss} period has been integrated and is ready to be applied to the model again. As a result, IOM modifies the number of on-time samples read by a HIL model. Consequently, the D values will alternate between adjacent quantized values. It keeps the same average value but possesses higher frequency components since it modifies the read D over fewer switching periods.

Fig. 6 depicts an extreme case in which a model without using IOM can read completely incorrect duty patterns just shifting the input, while including IOM leads to correct results. The number of samples per switching period is too low for a real application, but it helps to understand the principles of IOM. In this figure, the HIL model samples the input PWM signal with a resolution of $T_{ss} = 4T_{is}$ marked in red color ($N_{os} = 4$). T_{sw} and its on-time (T_{on}) are assumed $8T_{is}$ and $2T_{is}$, respectively. The waveforms in red demonstrate the input read by non-oversampled HIL systems that may contain low-frequency components. In Fig. 6(a), the HIL model without using IOM reads the D of zero while it reads $D = 0.5$ when the input PWM is shifted slightly shown in Fig. 6(b). The duty cycle read by a HIL model without using oversampling methods would alternate between these two values when there is a tiny deviation in T_{sw} value resulting in low-frequency aliasing oscillations. However, the green waveforms, which are the final signals sent to the HIL model using IOM, are not affected by the input shifting. The signals in orange are the F counters that have been used as internal signals in IOM. They count up every T_{is} if the original input signal is at a high level. They reset to zero when they reach $N_{os} = 4$. The falling edges of these signals are used as the trigger for the I signals depicted in blue. In this example, I is equivalent to 4 fractions. So when $I = 0$ and $F = 3$, and there is a new fraction, the method resets F to zero and increases I value as $I = 1$ is equivalent to $F = 4$. The HIL model using IOM will read I signal every T_{ss} resulting in the green waveforms. As can be seen in Fig. 6, shifting the input signal does not affect the model using IOM. In this figure, the signals in purple represent the input signals that an ideal oversampled HIL model can read (T_{ss} equals the T_{is} without suffering from the aliasing issue). Of course, it is not possible in HIL systems since the input sampling period is smaller than the minimum latency of the system for executing the model equations.

The main idea that has been used in IOM is to avoid a long periodic pattern of the read PWM signal by sampling it with a higher resolution. The average of the read input signal over time with or without IOM inclines toward the original input average value, considering that the latter avoids accumulating the error over time. Notably, the elimination of the switching low-frequency components by IOM does not come for free. Implementing this method in HIL systems increases the needed hardware resources. However, the extra hardware is negligible compared with the hardware demanded to implement the HIL systems

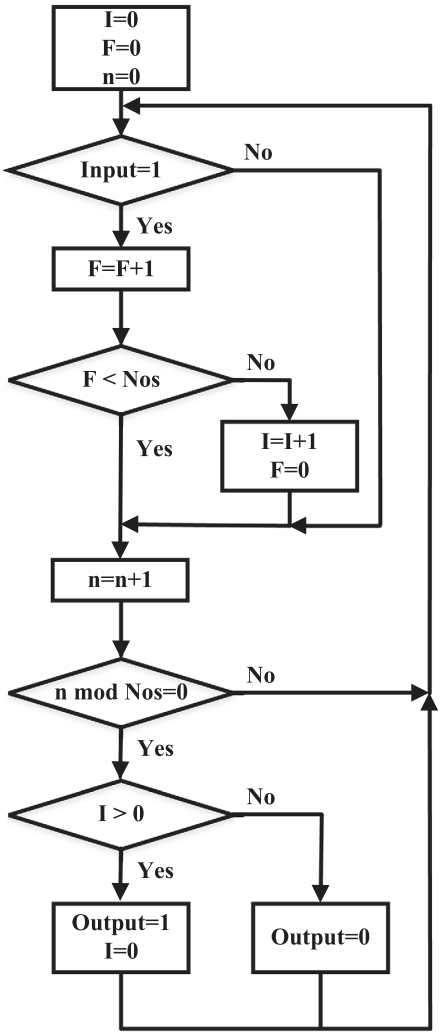

Fig. 5. Integration oversampling method flowchart.

in an FPGA. Using IOM, the rest of the HIL system, including the simulation time-step, remains unmodified, making it an ideal solution to prevent aliasing distortion found in HIL systems. IOM is easy to implement in an FPGA, and it can be easily integrated in the same FPGA in which the HIL model has been implemented. It also increases the effective resolution of the HIL system since the model can reach values between quantized values. Furthermore, no event correction is needed since the input transitions reformed by the IOM are in synchronism with the model T_{ss}. To the best of the authors' knowledge, IOM is the only solution for HIL switched models that use only one sample per simulation step. The input sampling frequency must be as high as possible to get the benefit of the IOM. Even if the above condition is

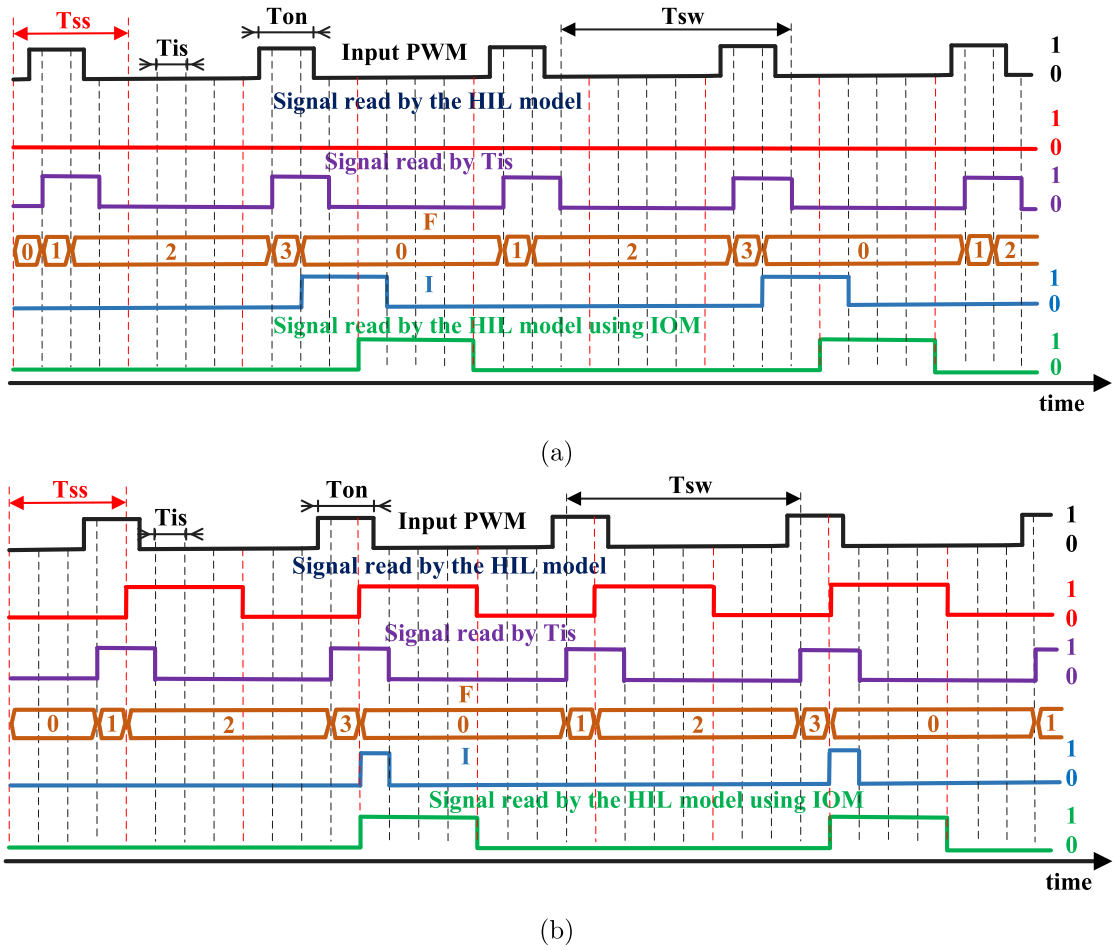

Fig. 6. Switching waveforms read by HIL models using different methods; (a) $T_{sw} = 8.T_{is}$, $D = 0.25$, (b) The same signal with a different initial phase.

met, aliasing distortion can still be seen in the output. However, the amplitudes of the oscillations decrease drastically, as will be shown in Section 5.

5. Simulation and experimental results

The higher fidelity of IOM over the model not using oversampling has been verified first by offline MATLAB simulations, then by experimental results. The experimental results have been obtained by implementing the idea in a low-cost commercial HIL setup, NI myRIO, with a Xilinx FPGA device (Xilinx Zynq-7010). The performance of IOM is evaluated by using a time-step of 500 ns (a commercial T_{ss}) and an input sampling of T_{is} = 25 ns. It is notable that the NI MyRIO device does not allow a further decrease in the input sampling period because the clock is set at 40 MHz and cannot be freely configured. However, it is enough to alleviate the aliasing oscillations, as shown in this section. Notably, most FPGA-based platforms support higher input sampling resolution (i.e. 3.5 ns [32]). So, the same idea can be implemented in other platforms using a higher sampling frequency. Of course, the higher the sampling frequency, the better results. However, even with a low sampling frequency of 40 MHz, the improvement in the results is clear, showing the validity of the method.

In order to properly compare the obtained results, four models are used in the comparison. Of course, all of them represent the same boost converter with the parameters of Table 1, using the same D and T_{sw} in each experiment. Two of the models are both simulated and tested in experimental results, while the other two are only simulated because they represent ideal behaviors non-reachable in RT. These four models are summarized in Table 2. The first ideal model is called "reference" and uses $T_{is} = T_{ss} = 1$ ns. In that way, there is no error in the input sampling, so model "reference" would be equivalent to an offline simulation with no sub-harmonics. The second model is called "ideal oversampling" and uses $T_{is} = T_{ss} = 25$ ns. Since the input sampling period will also be $T_{is} = 25$ ns for the experimental results, using $T_{ss} = 25$ ns implies using all the information from the input oversampling immediately. That is the best behavior that ideally could be obtained through oversampling. However, $T_{ss} = 25$ ns is unreachable in RT for the used platform, so this model will be only simulated as a comparison of the best behavior that could theoretically be achieved using oversampling at $T_{is} = 25$ ns. The third model is the proposed IOM model, called "IOM", which uses $T_{is} = 25$ ns and $T_{ss} = 500$ ns. The fourth model is a switched model without using IOM or any other oversampling technique, called "no oversampling", but using the same T_{ss} as the model "IOM". Therefore, the "no oversampling" uses $T_{is} = T_{ss} = 500$ ns. The third and fourth models are both simulated and checked through experimental results in the NI MyRIO platform. The expected result is that the "IOM" model has a behavior in between "ideal oversampling" and "no oversampling". If the behavior is closer to "ideal oversampling" than to "no oversampling" it would mean that the proposed IOM technique would be a valid technique for using oversampling while minimizing the impact on hardware resources.

As explained before, IOM modifies the D pattern read by the HIL model to avoid low-frequency components produced by input sampling. Fig. 7 shows the D read by different models. Although the "IOM" (the green signal) cannot achieve the original duty cycle's exact value (D = 0.42), it alternates the read D between adjacent possible values with a higher frequency. The zoomed plots of the effective D are depicted in the right part of Fig. 7 to reveal more details of its alternation using

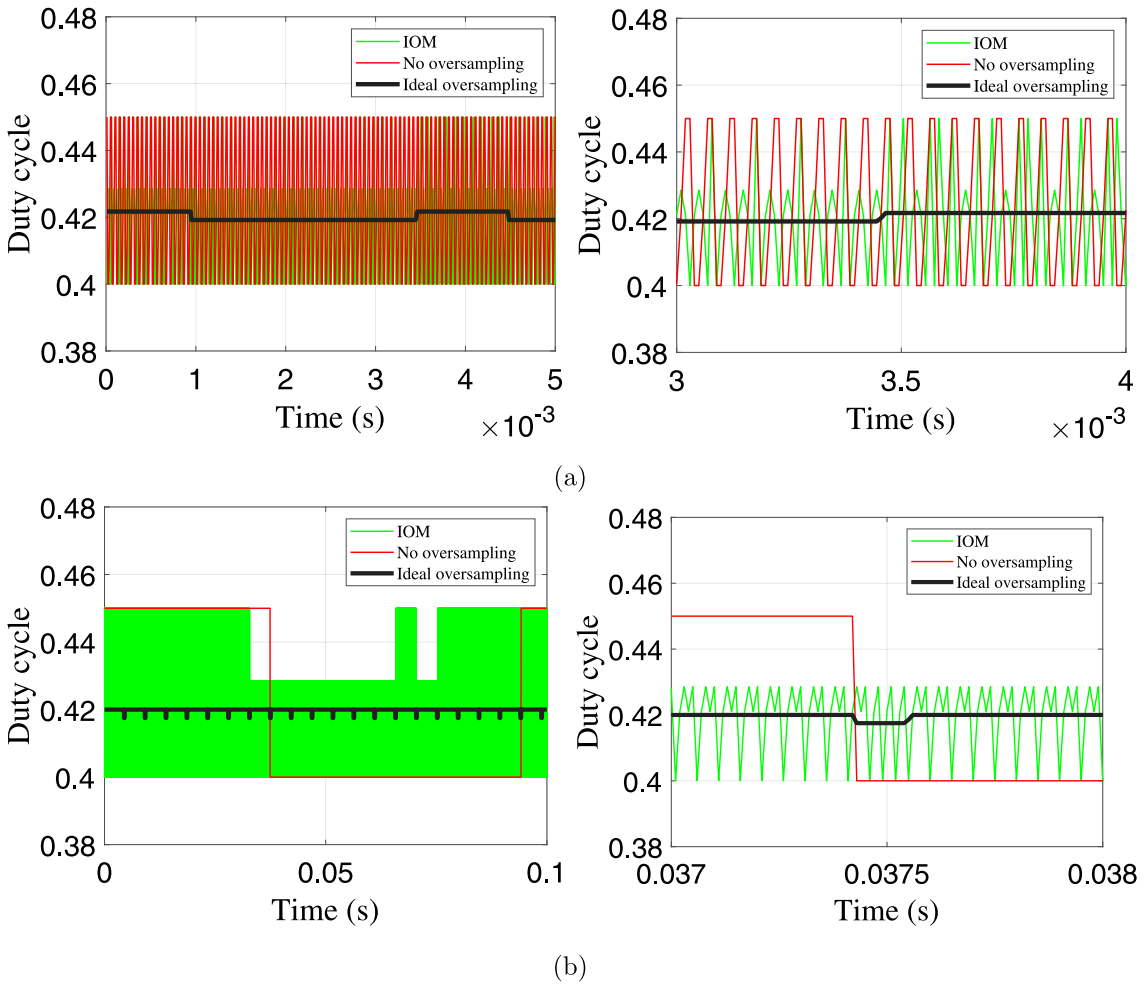

Fig. 7. The duty cycle pattern read by HIL model using different methods at T_{ss} = 500 ns & T_{is} = 25 ns & D = 0.42 (zoomed plots are shown in the right side); (a) T_{sw} = 9899.93 ns, (b) T_{sw} = 9999.947 ns.

Table 2
Summary of the tested models.

Model	T_{is}	T_{SS}	Test type
Reference	1 ns	1 ns	Sim
Ideal oversampling	25 ns	25 ns	Sim
IOM	25 ns	500 ns	Sim/Exp
No oversampling	500 ns	500 ns	Sim/Exp

different models. The D read by the "ideal oversampling" is depicted in black. Of course, T_{ss} of 25 ns cannot be obtained in RT. However, it is used as a reference that represents the ideal oversampling behavior.

The spectra analysis illustrated in Fig. 8 shows a significant reduction in the low-frequency aliasing sub-harmonics using IOM compared with the model without oversampling ("no oversampling"). The results are nearly the same as the results obtained by the "ideal oversampling" (the black signals with a T_{ss} of 25 ns). Despite the "no oversampling", the "IOM" steady-state inductor current plot, depicted in Fig. 8(c), tracks the "reference" waveform with less distortion. This figure proves that the HIL models using IOM can diminish the spurious steady-state oscillations caused by the sampling process. Furthermore, it shows that the performance of "IOM" is almost the same as "ideal oversampling". The same simulation results are shown in Fig. 9 to reveal the performance of IOM for the cases with a longer periodic pattern of D. As it can be seen, the advantage of using IOM is much higher in those cases.

Apart from the steady-state analysis, the accuracy of the HIL model dynamic response is also vital for checking the controllers' performance during a transient. As depicted in Fig. 10, the HIL model using IOM is overlapped with the "reference" and "ideal oversampling" waveforms in the transient state. As a result, IOM can be accepted as a solution to suppress the aliasing sub-harmonics and to enhance the HIL model precision without changing the model T_{ss}.

After evaluating the MATLAB simulations, the boost model is integrated into an NI myRIO device through LabVIEW, a graphical commercial tool from NI Company. The maximum sampling frequency in this device is 40 MHz due to the NI myRIO's FPGA clock period, which is 25 ns. The implemented model has a T_{ss} of 500 ns, so the model using IOM can read 20 samples within every T_{ss}. Fig. 11 verifies that the aliasing oscillation can appear even if the T_{sw} is a multiple of T_{ss} (T_{sw} = 10 000 ns). A small error in the T_{sw} due to the differences between the ideal and measured values will lead to steady-state oscillations, as supported by the simulation results. These high amplitude oscillations confuse the controllers since they cannot distinguish between the transient-state and steady-state. Fig. 11 shows how "IOM" can increase the effective output resolution of the model in open-loop tests resulting in aliasing oscillation attenuation.

A transient of the input D is shown in Fig. 12, while the rest of the parameters were kept constant. In this figure, the D is modified from 0.42 to 0.48 to demonstrate the dynamic response of IOM. As can be seen, the "no oversampling" inductor current transition is not identifiable. Thus, the HIL system using IOM can better reflect the dynamic behavior of the controller apart from its precise steady-state results. Other than minor steady-state oscillations, "IOM" achieves

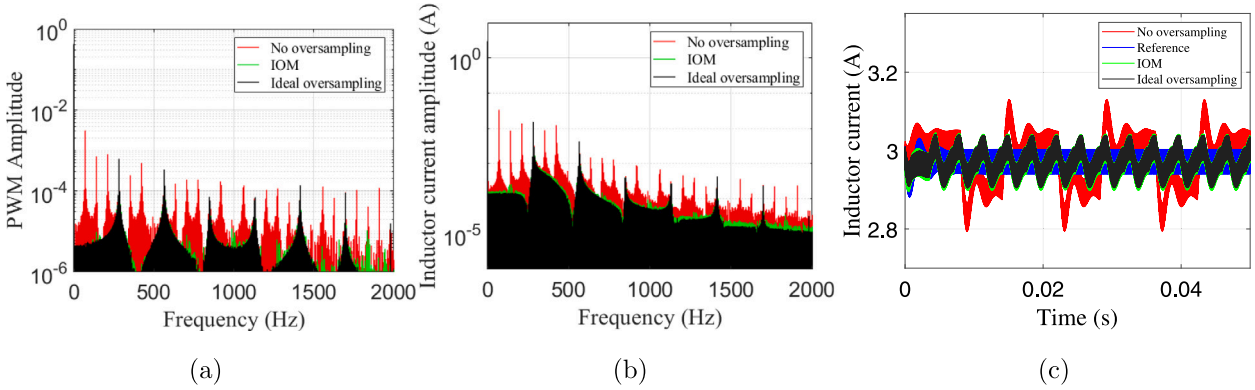

Fig. 8. The aliasing analysis of the HIL model at T_{sw} = 9899.93 ns & T_{ss} = 500 ns & T_{is} = 25 ns & D = 0.42; (a) The spectra analysis of the gate firing signal read by HIL model, (b) The spectra analysis of the inductor current, (c) The inductor current.

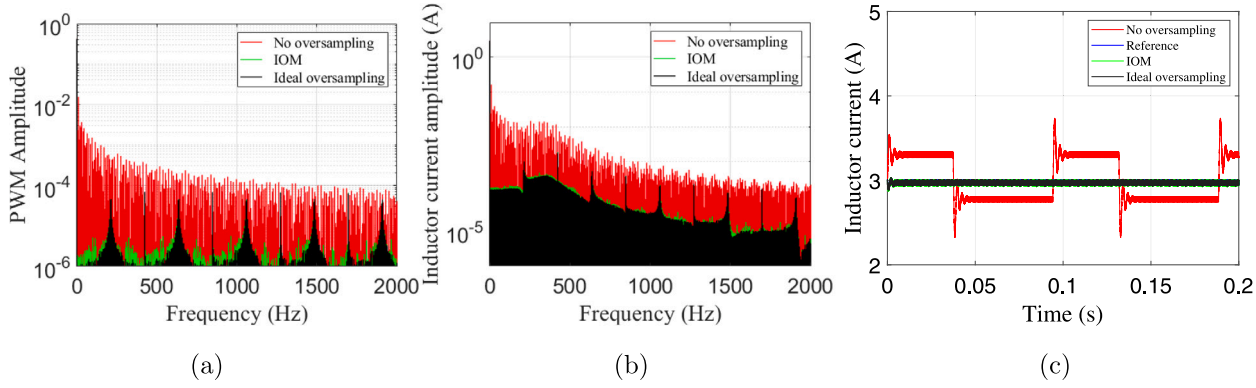

Fig. 9. The aliasing analysis of the HIL model at T_{sw} = 9999.947 ns & T_{ss} = 500 ns & T_{is} = 25 ns & D = 0.42; (a) The spectra analysis of the gate firing signal read by HIL model, (b) The spectra analysis of the inductor current, (c) The inductor current.

stable outputs in close agreement with the actual boost converter response.

Fig. 13 illustrates the HIL model response to the step-change provided by the user in the inductor current reference from 3 A to 4 A when the model is tested in closed-loop. First of all, the model is connected to a slow PI controller with a bandwidth of 5.31 Hz. Its transfer function is given as (7). The aliasing issue creates significant discrepancies, as shown in Fig. 13(a), that confuse the PI function. The results with a faster PID controller (see (8)) with a bandwidth of 1.05 kHz is demonstrated in Fig. 13(c). It proves that even fast controllers may suffer from the aliasing distortion, although the problem is less significant compared with the slow controllers. As depicted in Fig. 13, IOM improves the accuracy of the HIL model in the closed-loop test. Using IOM, the HIL model can test the controller function in both transient and steady-states even when the T_{ss} is relatively close to the T_{sw}.

$$R_{PI}(z) = \frac{0.002 - 0.0019z^{-1}}{1 - z^{-1}} \tag{7}$$

$$R_{PID}(z) = \frac{2 - 3.938z^{-1} + 1.939z^{-2}}{1 - z^{-1}} \tag{8}$$

Apart from steady-state and dynamic behavior, synthesis results are also analyzed to check the impact of the proposed method on necessary resources (area). Table 3 demonstrates that the model using IOM occupies nearly the same FPGA resources as the "no oversampling". The usage percentages of the resources are shown in the brackets for both implemented models. As can be seen, the "IOM" uses more slice registers and look-up tables (0.4% and 2.1%, respectively). The differences in a more complex HIL system could be even less since the additional resources needed for implementing IOM remains unchanged, irrespective of the model complexity.

Table 3
The synthesis results of the HIL model implementation into an NI myRIO device.

Sampling method	Slice registers	Slice LUTs	DSPs
No oversampling	11 618 (33%)	11 622 (66%)	76 (95%)
IOM	11 769 (33.4%)	11 981 (68.1%)	76 (95%)

6. Conclusion

This paper has presented a new oversampling method for HIL simulation of power electronic converters to alleviate the input sampling-induced aliasing oscillations. The proposed integration oversampling method (IOM) can be applied to the switched model of power converters. It avoids error accumulation by oversampling the input signal with a frequency higher than the simulation step. It dynamically modifies the input D during simulation time based on the input sampling error detected by oversampling the input signal. IOM was tested on a boost converter HIL model under open-loop and closed-loop configurations. The results confirmed the theoretical expectations, attenuating the aliasing oscillations. Compared with the HIL systems without using oversampling, IOM is less oscillatory and more accurate due to lower aliasing sub-harmonics entering the HIL model. IOM decreases three to nine times the inductor sub-harmonic oscillations compared with the model without any oversampling technique. More notably, the results obtained by IOM are almost identical to the ones obtained through ideal oversampling. However, the extra area needed for IOM is almost negligible, while other oversampling techniques have an important impact on area. Moreover, IOM has no impact at all on the necessary simulation step since IOM is just a block to be added between the input pin sampling and the input in the HIL model, while

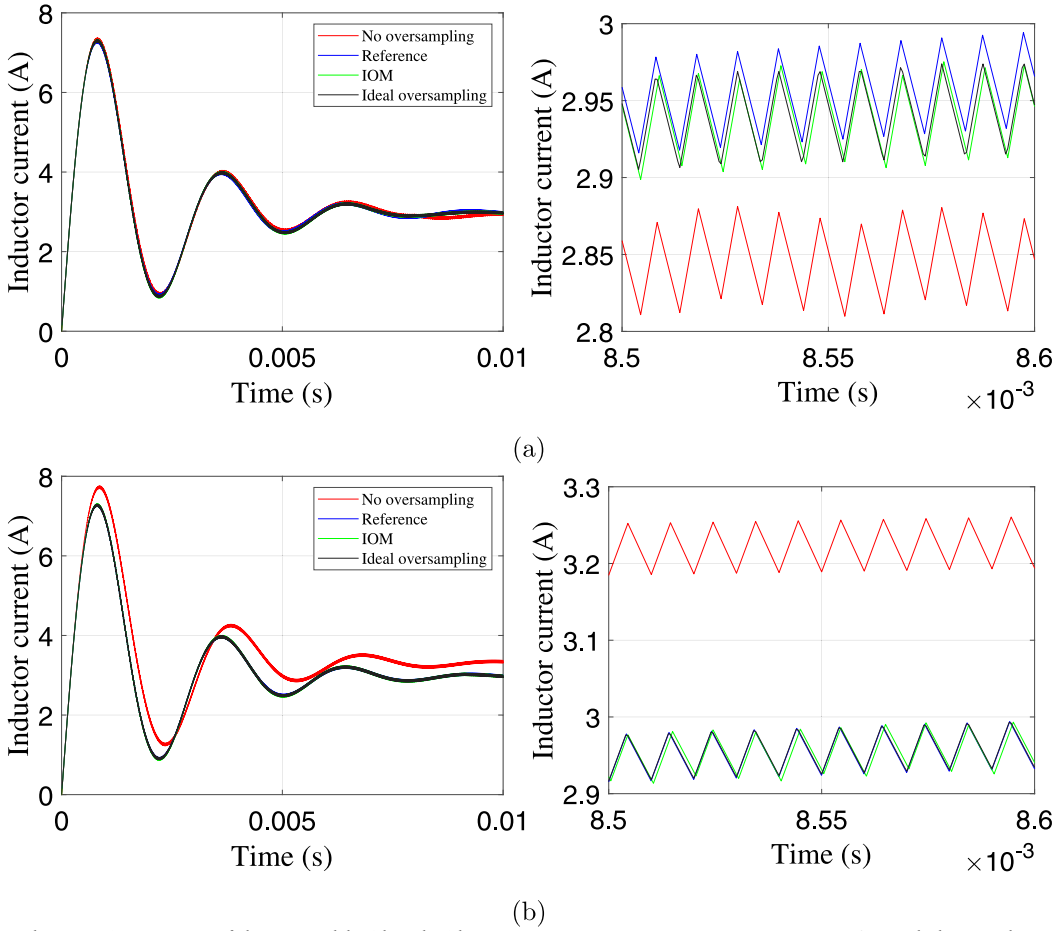

Fig. 10. Simulated open-loop transient response of the HIL model with and without IOM at $T_{ss} = 500$ ns & $T_{is} = 25$ ns & $D = 0.42$ (zoomed plots are shown in the right side); (a) $T_{sw} = 9899.93$ ns, (b) $T_{sw} = 9999.947$ ns.

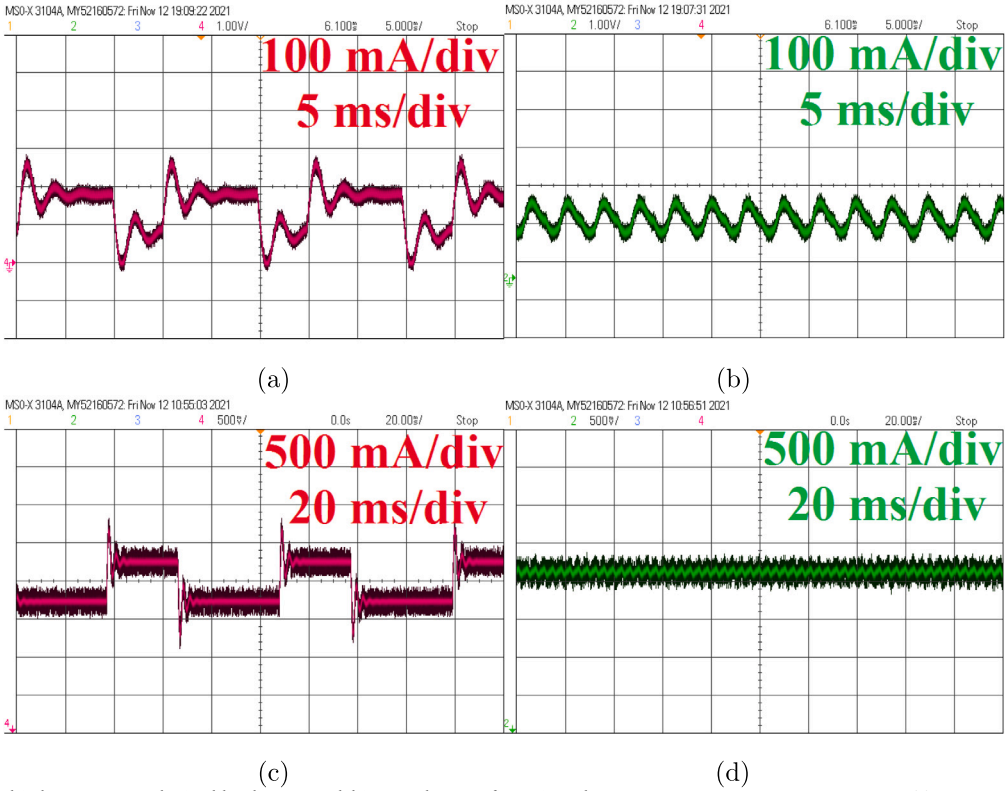

Fig. 11. The experimental inductor current obtained by the HIL model in open-loop configuration when $T_{ss} = 500$ ns & $T_{is} = 25$ ns & $D = 0.42$; (a) $T_{sw} = 9900$ ns, "no oversampling", (b) $T_{sw} = 9900$ ns, "IOM", (c) $T_{sw} = 10\,000$ ns, "no oversampling", (d) $T_{sw} = 10\,000$ ns, "IOM".

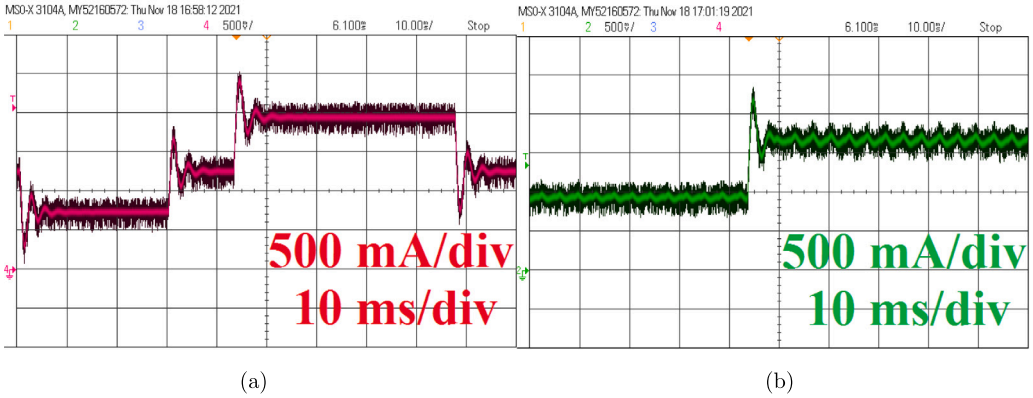

Fig. 12. Oscilloscope plot of the transient response of the inductor current obtained by the HIL model in open-loop when T_{sw} = 10 000 ns & T_{is} = 25 ns & T_{ss} = 500 ns & D = 0.42 *to* 0.48; (a) "no oversampling", (b) "IOM".

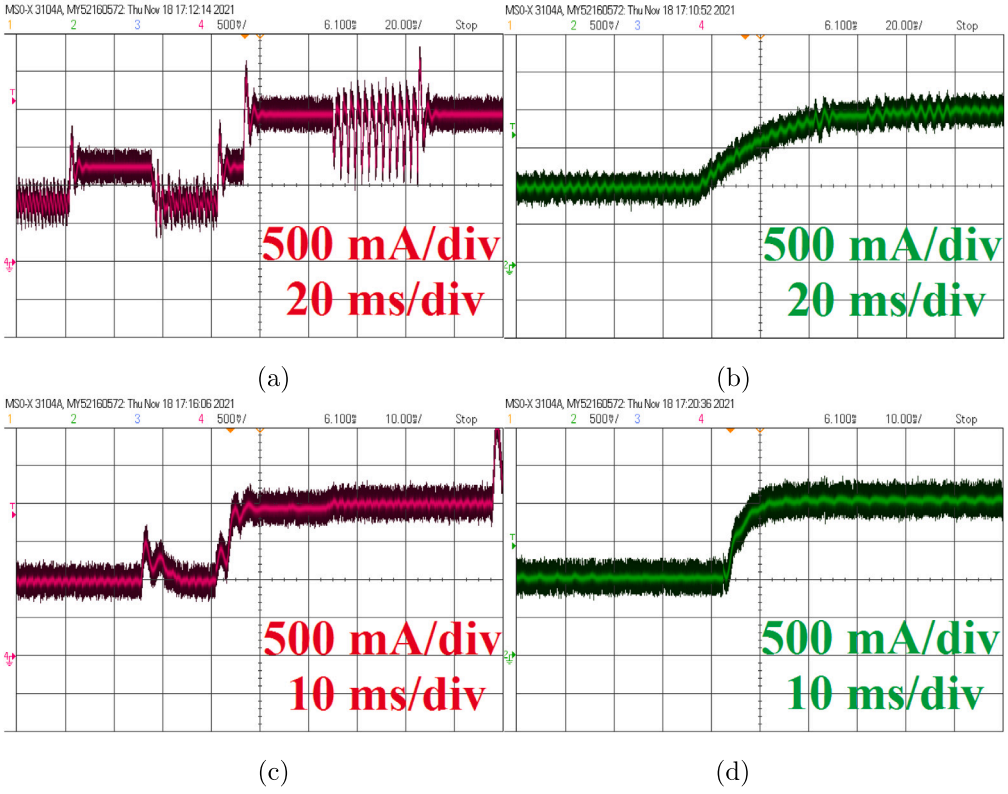

Fig. 13. Oscilloscope plot of the transient response of the inductor current in closed-loop when T_{sw} = 10 000 ns & T_{is} = 25 ns & T_{ss} = 500 ns & the inductor current reference is changed from 3 A to 4 A; (a) Disabling IOM with a slow controller, (b) Enabling IOM with a slow controller, (c) Disabling IOM with a fast controller, (d) Enabling IOM with a fast controller.

other oversampling techniques change the HIL model itself, increasing its complexity and therefore its simulation step. Finally, the increased output resolution achieved by IOM allows using longer simulation steps for high-frequency HIL applications where the simulation outputs become unacceptable when not using any oversampling technique.

CRediT authorship contribution statement

Elyas Zamiri: Conception and design of study, Acquisition of data, Analysis and/or interpretation of data, Writing – original draft, Writing – review & editing. **Alberto Sanchez:** Conception and design of study, Acquisition of data, Analysis and/or interpretation of data, Writing – original draft, Writing – review & editing. **María Sofía Martínez-García:** Conception and design of study, Acquisition of data, Analysis and/or interpretation of data, Writing – original draft, Writing – review & editing. **Angel de Castro:** Conception and design of study, Acquisition of data, Analysis and/or interpretation of data, Writing – original draft, Writing – review & editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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