



Four-period integration oversampling method (4PIOM) for hardware-in-the-loop power converters with complementary switches

Elyas Zamiri¹ · Alberto Sanchez¹ · Angel de Castro¹

Received: 10 July 2023 / Accepted: 9 February 2024
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Abstract

This paper addresses aliasing oscillations encountered in hardware-in-the-loop (HIL) simulation caused by inaccurate duty cycle detection in high-frequency power electronic applications. Oversampling has been commonly used as a solution to detect switching events more accurately. Traditional oversampling methods use the extra information obtained by oversampling the inputs for further computations to enhance the precision of the simulation. However, these techniques increase the complexity of the model since they take into account several switch states during each simulation step. To mitigate these complexities, the integration oversampling method (IOM) was introduced as a recent alternative with minimum impact on the model complexity. IOM provides a modified switching pattern that effectively prevents aliasing oscillations while maintaining a single switch-state for each simulation step. It can be implemented as an independent block between the controller and the HIL model, so it keeps the HIL model unchanged. This study highlights the limitations detected in applying IOM to the models with complementary switches, including possible undesired short circuits. To overcome these limitations, a novel oversampling method called 4PIOM is presented. 4PIOM further enhances the IOM algorithm by reducing the simulation step and sampling period. The validity of the new method is demonstrated by comparison with previous proposals and also with the same model without any oversampling. Both experimental and MATLAB simulation results prove its superior performance in attenuating the aliasing oscillations and improving the quality of the simulation.

Keywords Real-time simulation · Power electronics · Hardware-in-the-loop · Oversampling

List of symbols

4PIOM	Four-period integration oversampling method	$F\theta_1$	Fractional counter of state θ_1
ANPC	Active neutral point clamped	$F\theta_2$	Fractional counter of state θ_2
C	Capacitor capacitance	HIL	Hardware in the loop
D	Duty cycle	HSM	High Side Mosfet
F	Fractional counter in IOM	I	Integer counter in IOM
$f_{aliasing}$	Aliasing frequency	i_L	Inductor current
FHSM	Fractional counter of state HSM	ILA	Integrated logic analyzer
FLSM	Fractional counter of state LSM	IOM	Integration oversampling method
FPGA	Field-programmable gate array	L	Inductor inductance
		LCM	Least common multiple
		LSM	Low side mosfet
		N_f	Number of fractions in each T_{ss}
		R	Load resistance
		θ_1	First dead time
		θ_2	Second dead time
		T_{is}	Input sampling period
		T_{on}	ON time period
		T_{ss}	Simulation step
		T_{sw}	Switching period
		v_c	Capacitor voltage

✉ Elyas Zamiri
elyas.zamiri@uam.es

Alberto Sanchez
alberto.sanchezgonzalez@uam.es

Angel de Castro
angel.decastro@uam.es

¹ HCTLab Research Group, Universidad Autónoma de Madrid, Calle Francisco Tomás y Valiente 11, 28049 Madrid, Madrid, Spain

V_{in} Input voltage source

1 Introduction

Hardware-in-the-loop (HIL) simulation provides an efficient platform that is widely utilized in prototype development within power electronic applications, serving as a crucial step before proceeding to real-world tests. This approach allows for the comprehensive evaluation of a prototype's performance by connecting it to a real-time simulation of the rest of the system, as can be seen in [1, 2]. Thus, the behavior of the prototype can be checked under normal or extreme operating conditions that may be impractical or cost-prohibitive to replicate in power-level tests.

The core of HIL simulations relies on a real-time processor that facilitates the implementation of the model and analysis of interface signals. To further enhance the accuracy and reliability of HIL models, the traditional processor can be replaced by a field-programmable gate array (FPGA), a programmable hardware with ultra-low latency [3]. This is particularly beneficial for power electronic applications operating at high frequencies, exceeding 50 kHz. Studies such as [4–6] have emphasized the need for smaller simulation steps in such cases. In short words, the higher time resolution is, the more accurate and reliable is the HIL model [7]. However, even reaching simulation steps limited to hundreds of nanoseconds cannot guarantee the sufficient precision of the simulation, as highlighted in [8, 9].

The main challenge in HIL simulation of medium- to high-frequency converters is misdetection of the duty cycle when reading the control signals generated by the controller [8, 10]. In HIL simulations, the input sampling frequency, disabling oversampling methods, is the same as the HIL model frequency. When it is relatively close to the controller switching frequency (100 or fewer samples per switching period [4]), the error caused by the inaccurate reading of the duty cycle can be considerable and may lead to undesired steady-state oscillations known as aliasing oscillations [9]. Several oversampling methods have been proposed to achieve simulated signals that closely resemble the outputs of real converters.

Oversampling methods can be classified into three categories. In the first category, the model detects the transition moment by oversampling the input signals and then it recalculates the state variables when a switching event occurs. Variable simulation step [11] and inter/extrapolation methods [12, 13] belong to this group. While they offer higher accuracy, they also introduce greater complexity and increase the minimum possible simulation step. The second category includes time average [14, 15] and post-correction [16] methods. In this group, the idea is to calculate the average control signal and apply it to the average model of the converter. Thus, these methods are not applicable to switched models

of the converter. However, they are suitable for high switching frequency models where multiple switching events often happen during one simulation step. For example, a dual active bridge converter is taken as a case study in [8] to demonstrate the validity of the average method proposed by Typhoon HIL company. Integration oversampling method (IOM) presented in [17] does not belong to the previous categories. It enhances the accuracy of HIL simulation without modifying the HIL model. This approach can be implemented as an independent block that interfaces between the controller and the HIL model, significantly reducing the complexity level. However, as will be shown in this study, it cannot be applied to the converter models with complementary switches due to short-circuit problems arising from the complementary control signals.

This article first explains the short-circuit issue encountered in the application of IOM to the HIL model of a synchronous buck converter, serving as a case study. Subsequently, it introduces an adapted version of IOM named 4PIOM, designed to avoid this challenge while concurrently improving simulation precision. The superiority of the proposed method (4PIOM) above the rest of possibilities is discussed through accuracy analysis and a comparison of synthesis results. Furthermore, the study identifies scenarios where 4PIOM is indispensable and outlines its application to topologies with a higher number of components. In short words, this research significantly contributes to the field by mitigating aliasing oscillations and preserving HIL model simplicity, particularly in high-frequency power electronic applications.

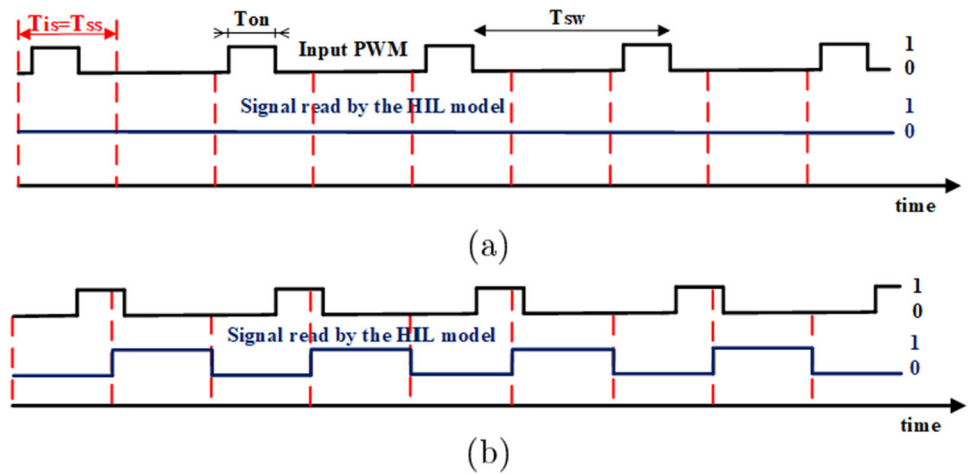
The rest of this paper is organized as follows: Section 2 presents an overview of aliasing oscillations caused by insufficient input sampling resolution, introduces IOM as a recent solution, and discusses its short-circuit problem. In Sect. 3, the 4PIOM method is introduced, along with a description of its priority logic. The precision results of the MATLAB simulation, experimental implementation, and synthesis results for implementing a synchronous buck converter are given in Sect. 4. Moving on, Sect. 5 delves into a comprehensive discussion, covering both the advantages and limitations of applying 4PIOM to HIL simulation of power converters. Finally, Sect. 6 concludes the article by summarizing the contributions of 4PIOM.

2 Aliasing oscillations in HIL systems

2.1 Aliasing issue

The main inputs in switching power converter HIL models that must be managed in real time are the gate signals sent to the gates of the switches (e.g., PWM inputs), which are digital inputs. Generally, simple HIL models read these inputs with

Fig. 1 Input PWM sampling in HIL systems without oversampling ($T_{is} = T_{ss}$); **a** $D = 0$ and **b** $D = 0.5$



a fixed period (T_{is}) equal to the period used for updating the model (T_{ss}), so $T_{ss} = T_{is}$. Despite the small T_{ss} s achieved by FPGA-based HIL models, they cannot detect the exact transition moments since the instants of switching events are not generally coincident with the clock of HIL models. It may cause aliasing oscillations that can be particularly observed in high-frequency tests of power converters when T_{is} is relatively close to the switching period. The solution is to decrease T_{is} without decreasing T_{ss} (oversampling). However, oversampling introduces additional information that, in general, must be processed by the model. Therefore, most oversampling methods increase the complexity and resources of the model significantly.

The concept of aliasing oscillations in discretized systems can be illustrated through an exaggerated example shown in Fig. 1. In this example, the sampled signals exhibit significant dissimilarity, despite a minor shift in the original PWM signal between the two subfigures. Of course, neither of the sampled signals accurately represents the PWM signal due to insufficient sampling resolution. In this scenario, $T_{ss} = T_{is}$ and T_{sw} corresponds exactly to $2T_{ss}$; however, $T_{on} = T_{ss}/2$. Therefore, the possible sampled signal D will be 0 or 0.5 (the original D is 0.25) depending on the initial phase of PWM signal. The aliasing problem arises when the sampled D alternates between these two adjacent values at a low frequency. Aliasing sub-harmonics can be calculated by (1), where LCM stands for the least common multiple and T_{is} represents the input sampling period. The low-frequency $f_{aliasing}$ will be the main source of the error in HIL simulation of power converters since the higher frequency will be naturally filtered by the converter.

$$f_{aliasing} = \frac{k}{LCM(T_{sw}, T_{is})}, \quad \text{for } k = 1, 2, 3, \dots \quad (1)$$

The concept of aliasing oscillations in HIL systems is addressed in [9] with more detail. According to the findings

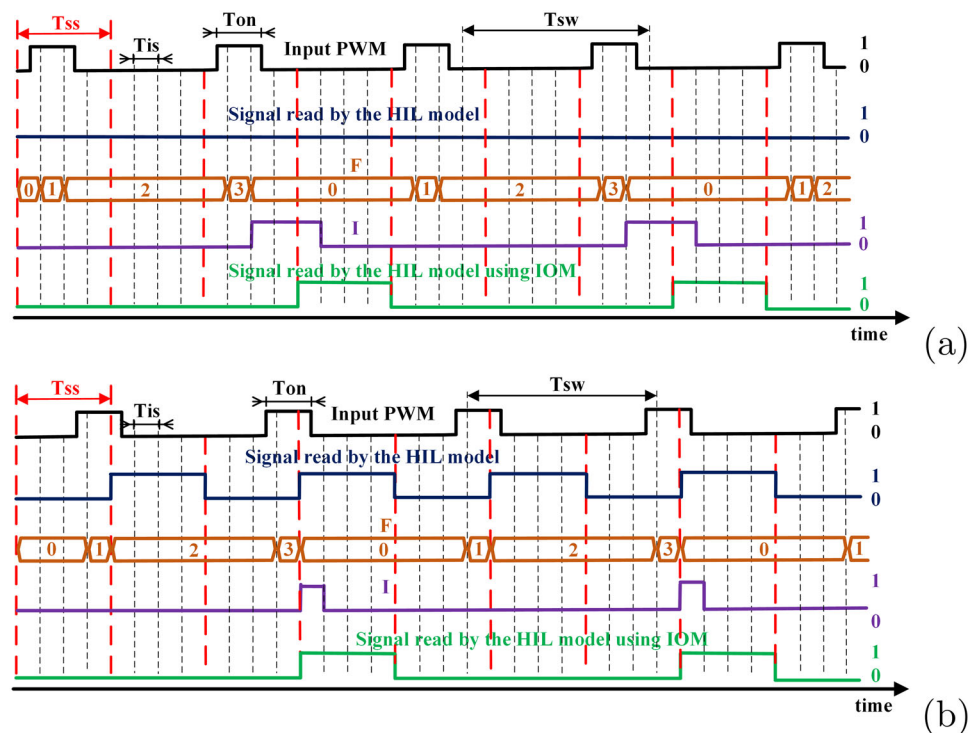
of that study, when T_{sw} is very close to an exact multiple of T_{is} , the HIL simulation will suffer from significant aliasing oscillations in steady state. For instance, a small change in T_{sw} from $T_{sw} = 2 T_{is}$ to $T_{sw} = 2.001 T_{is}$ in the example shown in Fig. 1 reduces the main aliasing sub-harmonic from $500/T_{ss}$ MHz to $0.5/T_{ss}$ MHz. As a consequence, the sampling instants shift slightly, leading to significant oscillations during steady state caused by the low-frequency alternation of D .

2.2 IOM algorithm [17]

A recent oversampling method, called IOM, has been presented in [17] to reduce the error associated with inaccurate reading of the duty cycle (D) in HIL models. The method is based on oversampling the gate signal but it does not compute the state variable at switching events instants as the other oversampling methods. IOM is easy to implement in FPGAs and can be implemented in a HIL system by adding a small hardware block between the actual gate signal and the gate input of the HIL model. This block generates a single gate signal value at every simulation step (on or off state when a mixed on/off is detected). Of course, there is an error only during gate transitions, when the gate signal is not just on or off during a whole simulation step. This error is integrated (i.e., accumulated), taking it into account for changing the following gate values that will be sent to the power converter model, in a similar way to the principle of sigma-delta modulators [18] or dithering technique [19].

IOM accumulates the fractions of on time until a complete T_{ss} is integrated, and then it applies the accumulated on time to the HIL model. Its performance is shown in Fig. 2. The number of fractions (F in orange) is incremented by 1 every time the gate signal is on (Input = 1) in a rising edge of the oversampling clock (T_{is}). When F reaches T_{ss}/T_{is} , the integer (I in purple) is increased in the form of a carry bit, and F starts over at 0. The auxiliary 1-bit I signal, generated

Fig. 2 Switching waveforms read by HIL models with and without IOM; **a** $T_{sw} = 8 \cdot T_{is}$, $D = 0.25$, **b** The same signal with a different initial phase



in the IOM, contains all the extra information obtained by the input oversampling. Whenever I is greater than zero, the method waits until the following simulation step rising edge and then applies a complete on T_{ss} cycle to the model. At this moment, I is reset from I to $I - 1$ since the integrated T_{ss} period has already been applied. This process will be repeated using IOM for each gate signal independently, irrespective of the power converter type.

Using IOM, the HIL model does not need to be reconstructed and all additional information obtained by oversampling the input signal will be handled inside the embedded IOM interface block. As justified in [17], IOM provides an appropriate set of gate signal values breaking the long periodic patterns that may happen due to the aliasing issue. Furthermore, no event correction is needed since the input transitions reformed by the IOM are in synchronism with the model T_{ss} . IOM is the only oversampling solution for HIL switched models that only uses one sample per simulation step. However, applying it directly to complementary gate signals can lead to short-circuit situations that will be highlighted in the following subsection.

2.3 Short-circuit problem in IOM

Although IOM is an efficient solution to attenuate aliasing oscillations in HIL simulations because of its simplicity, it cannot be directly applied to HIL models with complementary switches since it may cause short-circuit issues demonstrated in Fig. 3. The undesired short-circuit signifi-

cantly impacts the behavior of HIL models, so this technique is not recommended for converters with complementary switches (such as modular multilevel inverters, H-bridge inverter, synchronous buck converter, etc), especially if the dead time for their complementary switches is in the range of the model T_{ss} or lower.

IOM integrates the error in reading the input signal and applies the accumulated on time later when it reaches a complete T_{ss} . The delay in applying the on time can cause the short-circuit issue for complementary switches. For example, Fig. 3 shows two complementary signals in black color (HSM (high-side Mosfet) and LSM (low-side Mosfet)) that are oversampled by IOM. The green signals represent the modified signal generated by IOM block. It clearly shows how the delay in IOM outputs results in short-circuit issue. Of course, this is an extreme case with few number of samples in each switching period but the short-circuit situation is readily discernible in this figure.

3 Four-period IOM (4PIOM)

4PIOM is presented to overcome the short-circuit problem discovered in the previous section when applying IOM to complementary gate signals. Two complementary signals are shown in Fig. 4 that include four different switching states, HSM (HSM = 1 & LSM = 0), θ_1 (HSM = 0 & LSM = 0 & LHSM = 1), LSM (HSM = 0 & LSM = 1), θ_2 (HSM = 0 & LSM = 0 & LHSM = 0). LHSM represents the last switch

Fig. 3 Short-circuit problem caused by IOM for complementary switches

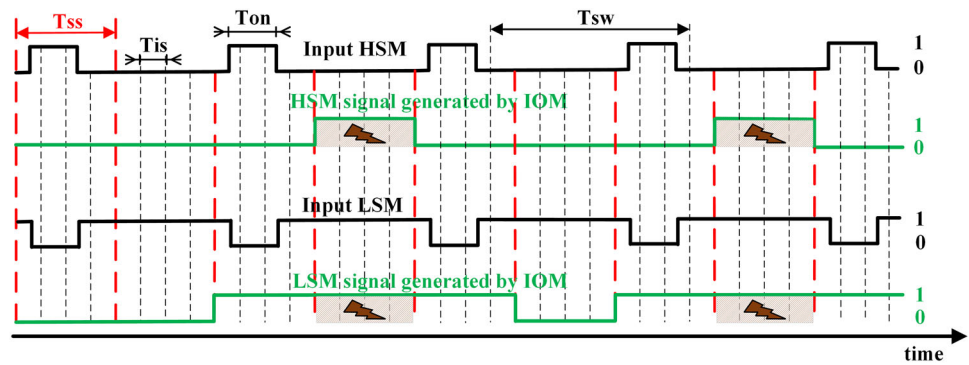
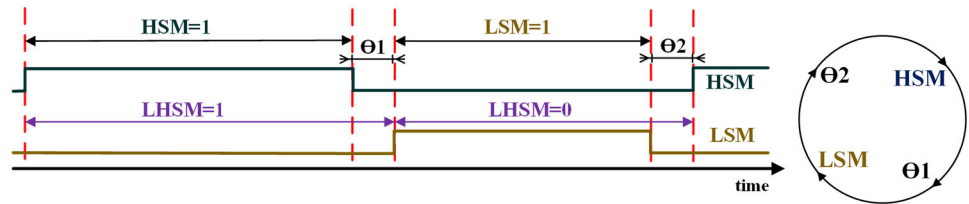


Fig. 4 Complementary signals considering dead time and the desired switching state sequence



that was on (1 for HSM, 0 for LSM), and it has been used for distinguishing between θ_1 and θ_2 , which are the two different dead times: θ_1 after HSM on, θ_2 after LSM on.

4PIOM oversamples the input signals with a frequency higher than T_{ss} and accumulates the time fractions for each state. The number of fractions (FHSM, F_{θ_1} , FLSM, and F_{θ_2}) are incremented by 1 every time the correspondent state is detected by a rising edge of the T_{is} clock. 4PIOM decides whether to apply HSM, θ_1 , LSM, or θ_2 state at every rising edge of T_{ss} with respect to the accumulated fractions. 4PIOM block applies the state with greater integrated time, taking into account the sequence of the signals shown in Fig. 4. For example, θ_1 cannot be selected when the last generated state is LSM even if F_{θ_1} is greater than the other fractional counters. Right after deciding about the correct state at each simulation step the equivalent fractional counter will be decreased by $N_f = T_{ss}/T_{is}$ (the number of fractions in a complete simulation step). Thus, the sums of the fractional counters cannot exceed N_f at any moment. The 4PIOM principles to decide the next switching state are simplified in the following sequence, and several cases with different values of fractional counters as examples are given in Table 1.

1. θ_1 and θ_2 will be generated only after HSM and LSM states, respectively. Thus, 4PIOM will not apply them to the output if they do not follow the sequence shown in Fig. 4. For instance, when the input switching state is HSM, the output cannot be in θ_1 state.
2. 4PIOM will generate the output state corresponding to the greater fractional counters at every simulation step, if the previous rule is not broken. If not, the second greater counter is chosen.

3. If there is a tie between two or more fractional counters, then the 4PIOM will generate:

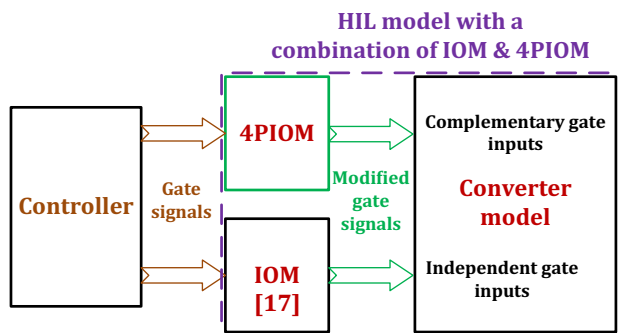
- The previous output state if the correspondent fractional counter is in the tie.
- The next output state based on the switching state sequence if the correspondent fractional counter is in the tie.
- The state after next if the correspondent fractional counter is in the tie.

Table 1 demonstrates several cases with different values of fractional counters as examples in which the performance of 4PIOM can be seen. The values of fractional counters are represented at the rising edge of T_{ss} with $N_f = 40$. These counters have been used as internal signals to decide about the next state following the principles presented before. They are subtracted from N_f when 4PIOM applies them to the output (the final signals sent to the HIL model). Cases 1 and 2 demonstrate that 4PIOM applies HSM or LSM state if the greatest counter is FHSM or FLSM, respectively. Case 3 demonstrates the 4PIOM output when F_{θ_1} is greater than the other counters. A similar condition is shown in case 4 when F_{θ_2} is the greatest fractional counter. Cases 5 to 8 provide some examples when there is a tie between two or more fractional counters.

The concept behind 4PIOM is designed to address the specific IOM challenge posed by each pair of complementary switches within a converter. Therefore, to facilitate a clear and concise analysis without introducing unnecessary complexities, a straightforward case study is conducted using a synchronous buck converter with only a pair of complementary switches. It is essential to note that 4PIOM is specifically designed for complementary switches. However, more com-

Table 1 4PIOM output based on the values of the fractional counters

Case	F_{HSM}	$F_{\theta 1}$	F_{LSM}	$F_{\theta 2}$	Current input	Previous output	4PIOM output	Action
1	50	-10	-20	-20	X	X	HSM	$F_{HSM} - N_f$
2	10	10	20	0	X	X	LSM	$F_{LSM} - N_f$
3	15	30	5	-10	HSM \neq HSM	X	HSM $\theta 1$	$F_{HSM} - N_f$ $F_{\theta 1} - N_f$
4	-5	5	15	25	LSM \neq LSM	X	LSM $\theta 2$	$F_{LSM} - N_f$ $F_{\theta 2} - N_f$
5	15	15	10	0	X	HSM $\theta 1$ LSM $\theta 2$	HSM $\theta 1$ HSM HSM	$F_{HSM} - N_f$ $F_{\theta 1} - N_f$ $F_{HSM} - N_f$ $F_{HSM} - N_f$
6	10	15	15	0	X	HSM $\theta 1$ LSM $\theta 2$	$\theta 1$ $\theta 1$ LSM $\theta 1$	$F_{\theta 1} - N_f$ $F_{\theta 1} - N_f$ $F_{LSM} - N_f$ $F_{\theta 1} - N_f$
7	15	10	15	0	X	HSM $\theta 1$ LSM $\theta 2$	HSM LSM LSM HSM	$F_{HSM} - N_f$ $F_{LSM} - N_f$ $F_{LSM} - N_f$ $F_{HSM} - N_f$
8	15	15	-5	15	X	HSM $\theta 1$ LSM $\theta 2$	HSM $\theta 1$ $\theta 2$ $\theta 2$	$F_{HSM} - N_f$ $F_{\theta 1} - N_f$ $F_{\theta 2} - N_f$ $F_{\theta 2} - N_f$

**Fig. 5** General block diagram of a HIL model incorporating 4PIOM

plex converters with several pairs of complementary switches can benefit from this technique by employing a 4PIOM block for each pair of switches. Additionally, it can be combined with regular IOM blocks, as depicted in Fig. 5, to be applied in converters that have both pairs of switches and also independent switches. Exploring the application of this method in other topologies with a higher number of components, such as multilevel converters, is a future research direction for this study, further validating its applicability in more complex case studies.

4PIOM avoids accumulating the error over time by oversampling the input signals in HIL models. In each simulation step, it effectively selects the switching state with the

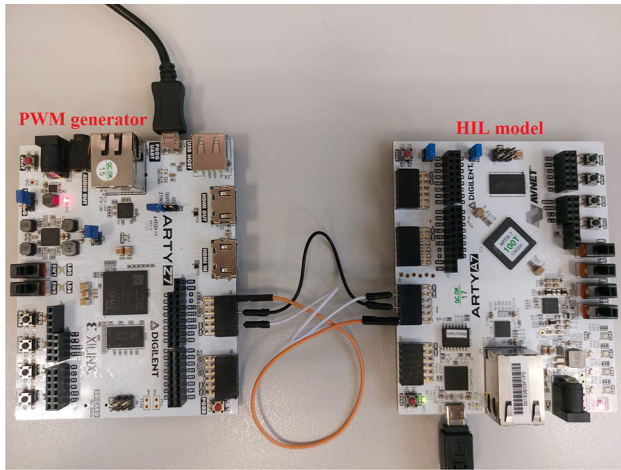
larger integrated error, while also considering the anticipated switching sequence in complementary switches. Compared with IOM, 4PIOM does not suffer from short-circuit problems in these cases. The critical advantage of eliminating unexpected short-circuit issues comes at the expense of a slightly more intricate algorithmic structure in the case of 4PIOM. However, the extra hardware resources required for its FPGA implementation remain negligible, particularly when compared to the hardware demands of HIL systems.

4 Simulation and experimental results

In this section, the higher fidelity of 4PIOM over models not using oversampling or models with conventional oversampling methods has been verified first by offline MATLAB simulations, then by experimental results. The experimental results have been obtained by implementing the proposed oversampling method and a discretized synchronous buck converter model (32-bit floating-point numerical format defined by the IEEE 754 standard) into a low-cost FPGA board (Xilinx Arty-A7). The nominal values of different parameters and the input signals are given in Table 2. The model interfaces with a pair of external complementary PWM signals, HSM and LSM, exhibiting a consistent duty cycle, along with two different dead times (θ_1 and θ_2).

Table 2 Simulation parameters of the synchronous buck converter

Parameters	Values	Parameters	Values
Input voltage	$V_{in} = 28 \text{ V}$	Switching period	$T_{sw} = 5000.05 \text{ ns}$
Inductor	$L = 20 \mu\text{H}$	HSM duty cycle	$D = 0.42$
Capacitor	$C = 60 \mu\text{F}$	Dead time 1	$\theta_1 = 24.0 \text{ ns}$
Capacitor voltage	$v_c \approx 12 \text{ V}$	Dead time 2	$\theta_2 = 72.0 \text{ ns}$

**Fig. 6** Experimental setup for HIL test

Notably, these PWM signals are generated by a separate FPGA board, specifically the Xilinx Artix-Z7-20, as shown in Fig. 6. This twin setup aims to closely emulate real-world conditions for HIL testing scenarios, with one FPGA board (Artix-Z7-20) generating the gate signals and therefore doing the role of the controller, and the other FPGA board (Artix-A7) running the HIL model. In the simulation test, the switching period is chosen 5000.05 ns to represent a realistic case for showing the aliasing issue caused by a small difference between the switching period and a perfect multiple of the input sampling step. However, the exact switching period will be different in experimental tests causing similar oscillations but with another frequency. The tests are accomplished with two different loads to demonstrate the performance of 4PIOM for low/high loads. In this section, the T_{ss} for the HIL model and the oversampling resolution are set to 200 ns and 5 ns, respectively. These numbers can be achieved easily in an FPGA-based HIL platform, as will be shown through experimental results.

The simulation results obtained by using 4PIOM highlight the advantages of the proposed oversampling method compared with the other possible solutions when the HIL model receives a pair of complementary signals. Four models are involved in the comparison study. The “Ideal oversampling” model represents the desired behavior of the simulation but it can be obtained only in offline simulations. It reduces the value of the T_{ss} to the input sampling step (5 ns), so it pro-

vides the highest precision. The second model is called “No oversampling” which uses $T_{is} = T_{ss} = 200 \text{ ns}$. The resolution of 200 ns is high enough to avoid aliasing issues in most HIL applications. However, it will be shown that significant oscillations may happen even reaching this small T_{ss} . The third model is based on the IOM model presented in [17]. In [17], it was implemented in an NI MyRIO FPGA board with a T_{ss} of 500 ns and a sampling period of 25 ns. However, to perform a fair comparison, it has been implemented in the Xilinx Artix-7 FPGA, using the same coding standards (hand-coded VHDL), reaching $T_{ss} = 200 \text{ ns}$, and $T_{is} = 5 \text{ ns}$. Finally, the fourth model is 4PIOM, which solves not only the short-circuit problem in IOM but also attenuates the aliasing oscillations in HIL simulations of power converters with complementary switches.

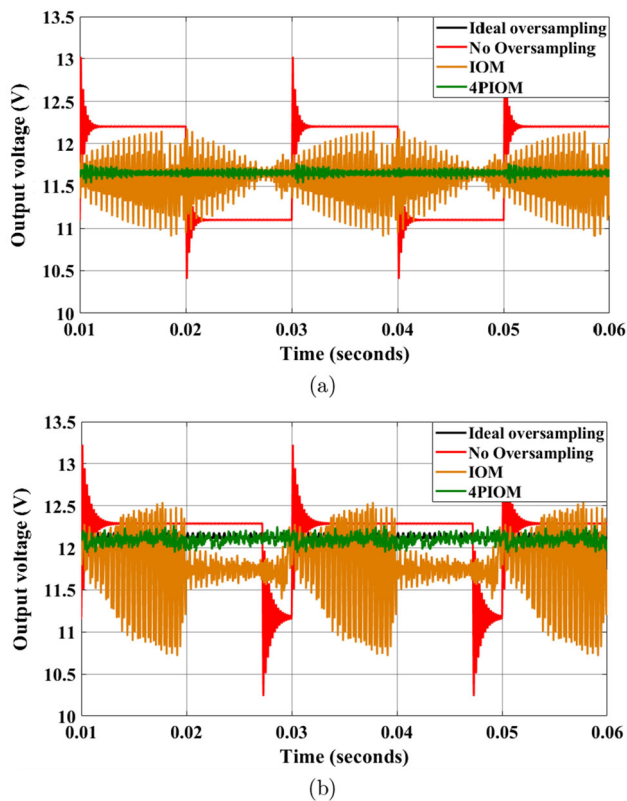
The following simulations and experimental tests focus on the steady-state capacitor voltage to clarify the error caused by the aliasing distortion using each method, but a similar analysis can be accomplished for the inductor current as the other state variable in this example. Figure 7 illustrates the MATLAB simulation results of the capacitor voltage in steady state for the discussed methods. As expected, the IOM model reduces the aliasing oscillations. However, it tracks a different offset value and the oscillations are still significant. The main reason is the short-circuit problem in the complementary gate signals, as explained before. Figure 7 verifies that 4PIOM provides an output very similar to the reference signal for both tested loads. This is because 4PIOM does not modify the average values of dead times. The incorrect θ_2 average value would cause an offset error in the output when the inductor current reaches negative values. If the inductor current is always positive, this error will not change the equations of the circuit, as can be seen in (2).

$$i_L(k+1) = i_L(k) + \frac{T_{ss}}{L} \cdot \begin{cases} V_{in} - v_c & \text{HSM or } \theta_1 \& i_L < 0 \text{ or } \theta_2 \& i_L < 0 \\ -v_c & \text{Others} \end{cases} \quad (2)$$

Three main criteria are involved to compare the performance of the discussed oversampling methods. The first criterion is the mean absolute error of the output signal, in this case the capacitor voltage. The second one is the output average value to check if the simulation suffers from an

Table 3 Capacitor voltage error analysis in steady state using different methods

Model Load (Ω)	Mean absolute error		Average error		Peak-to-peak oscillations	
	5	18	5	18	5	18
No oversampling	4.76%	2.55%	−0.05%	−0.018%	2.65 V	2.95 V
IOM [17]	1.62%	4.85%	−1.52%	−4.75%	1.2 V	1.8 V
4PIOM	0.08%	0.15%	−0.04%	−0.015%	0.09 V	0.11 V

**Fig. 7** Output voltage obtained by 4PIOM vs IOM and “No oversampling”, $T_{sw} = 5000.05$ ns, $D_{HSM} = 0.42$, $\theta_1 = 24$ ns, and $\theta_2 = 72$ ns; **a** Positive inductor current $R = 5 \Omega$ **b** $R = 18 \Omega$

offset error in steady state. And finally, the third criterion is the peak-to-peak steady-state oscillations. It is even more important than the offset error since HIL models are usually employed to test the dynamic and steady-state behavior of the controllers. When there are significant aliasing oscillations, the user cannot distinguish between the transient and steady-state response of the controller. The comparison between different methods based on these criteria is presented in Table 3. As calculated in this table, 4PIOM attenuates the steady-state oscillations caused by aliasing issue better than IOM. Furthermore, IOM suffers from a higher percentage of offset error for low-load simulation ($R = 18 \Omega$).

The functionality of 4PIOM is also verified experimentally by implementing the complementary signal generator and the HIL model into two separate FPGA boards. Each board has its own internal clock, so the aliasing problem may

happen. In this test, the state variables of the HIL model are only sampled at every simulation step of 200 ns by reading the complementary signals generated by 4PIOM. It oversamples external gate signals with a period of 5 ns. The model output voltage with and without 4PIOM are captured using ILA (integrated logic analyzer) IP core in Vivado, as illustrated in Fig. 8. It takes a sample every two switching periods (every sample is equivalent to $10 \mu s$) and the output voltage amplitude is converted to decimal, as can be seen in this figure.

Apart from the HIL simulation precision, synthesis results are also compared to check the impact of the each method on necessary hardware resources. In case of the synchronous buck converter, the number of LUTs are 37890, 39100, and 41509 in “No oversampling,” “IOM,” and “4PIOM,” respectively. All methods need the same number of DSPs (20), and their minimum achievable clock periods are almost the same (148 ns). The synthesis results obtained by Vivado prove that 4PIOM demands higher hardware resources compared with other approaches. However, the extra hardware resource is negligible, while it allows for correctly tracking the behavior of the converter without considerable offset error or aliasing oscillations.

5 Discussion

The proposed 4PIOM block is an oversampling technique similar to IOM, but specifically designed to be applied to pairs of complementary switches. Both can be seamlessly integrated as external blocks between the gate inputs generated by the controller and the HIL model in HIL setups. These blocks receive high-frequency sampled switching pulses, aiming to deliver these signals to the pre-designed HIL model of switching converters without requiring any modifications to the model itself. Keeping the HIL model without modifications is the key advantage of IOM/4PIOM with respect to other classical oversampling methods. Furthermore, the extra hardware resources needed for implementing these blocks are negligible when compared with the resources required for the HIL model of switching converters. Despite these advantages, IOM/4PIOM introduce a slightly higher delay than the traditional oversampling methods [12, 20, 21]. This extra delay may alter the instantaneous behavior of the HIL model. However, as demonstrated in Sect. 4, the achieved

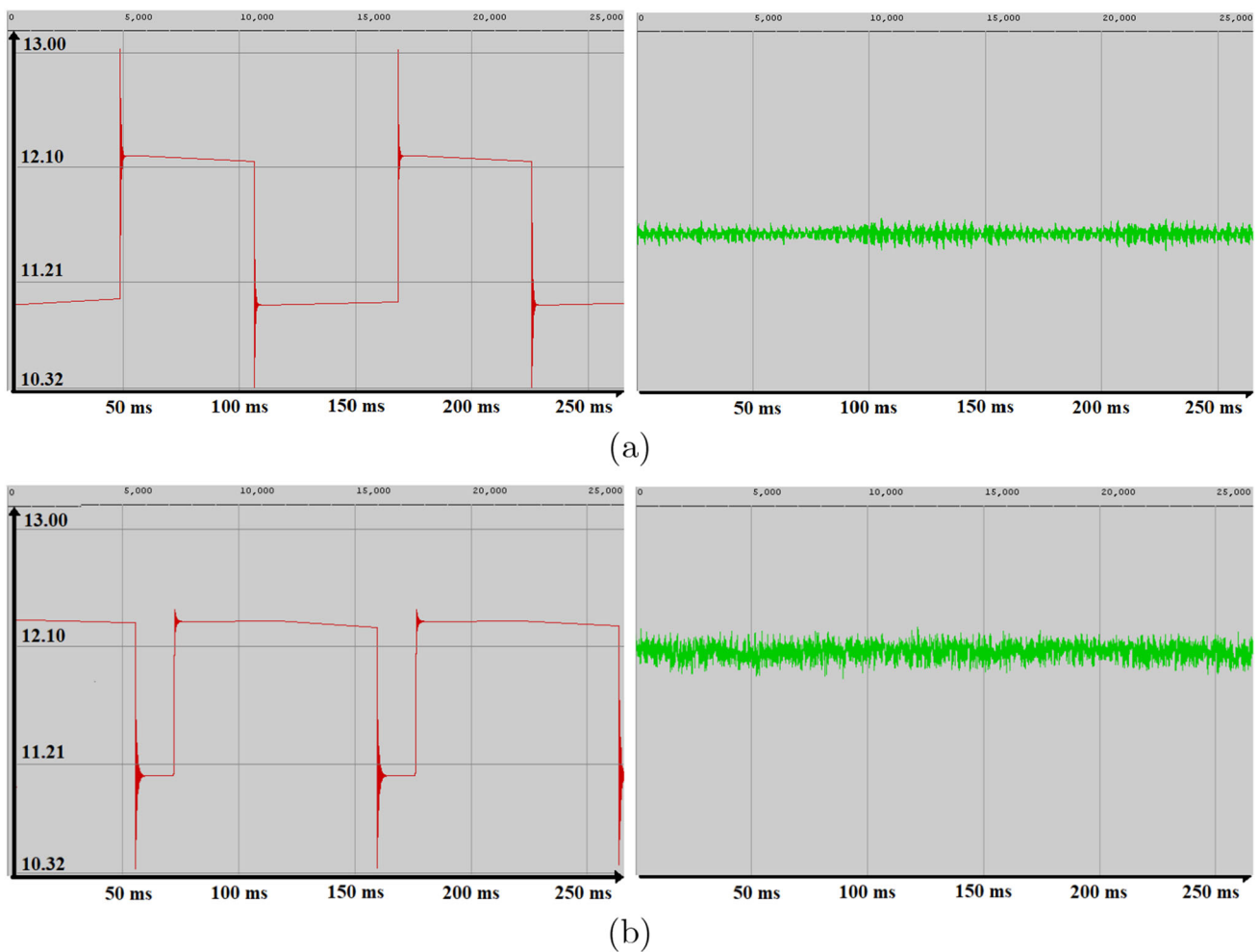


Fig. 8 Output voltage obtained by experimental test, 4PIOM (in green) vs “No oversampling” (in red), $T_{sw} = 5000$ ns, $D_{HSM} = 0.42$, $\theta_1 = 24$ ns, and $\theta_2 = 72$ ns; **a** Positive inductor current $R = 5 \Omega$ **b** $R = 18 \Omega$ (color figure online)

results for 4PIOM show a remarkable similarity to the ideal oversampling method for 4PIOM. A similar observation is reported by Zamiri et al. [17] for IOM.

Apart from the similarity between IOM and 4PIOM, the latter resolves a specific problem detected in IOM. When IOM is applied to pairs of complementary switches, it may lead to a short-circuit issue within the HIL model, likely when the dead time is short. While the short-circuit problem in HIL models is not as critical as in physical tests, it can introduce offset errors and significant oscillations during HIL simulations. These challenges are effectively addressed by 4PIOM, as demonstrated in Sect. 4. Furthermore, although the algorithm of 4PIOM is slightly more complex than IOM, the additional complexity remains negligible when compared to the overall complexity of the HIL model.

4PIOM is introduced only for pairs of complementary switches. In applications involving multiple pairs of complementary switches, it necessitates the integration of additional 4PIOM blocks. Each of these blocks corresponds to a spe-

cific pair of complementary switches. For instance, in a three-phase active neutral point clamped (ANPC) converter depicted in Fig. 9, integrating three 4PIOM blocks is needed for each phase. In this case study, switches Q_1 , Q_2 , and Q_5 are complementary to Q_4 , Q_3 , and Q_6 , respectively, indicating that they cannot be ON simultaneously. Consequently, Q_1 and Q_4 are connected to one 4PIOM block, Q_2 and Q_3 to another, and Q_5 and Q_6 to a third block. This integration of 4PIOM blocks extends to the other two phases in this example, resulting in employing nine 4PIOM blocks, as can be seen in Fig. 9. Notably, this figure emphasizes that the original HIL model remains unmodified even in cases with multiple pairs of complementary switches. It is worth noting that this method offers the flexibility of being combined with IOM in converters that incorporate both individual switches and pairs of complementary switches, as previously demonstrated in Fig. 5.

The choice of an appropriate oversampling method in HIL simulations depends on factors such as the application fre-

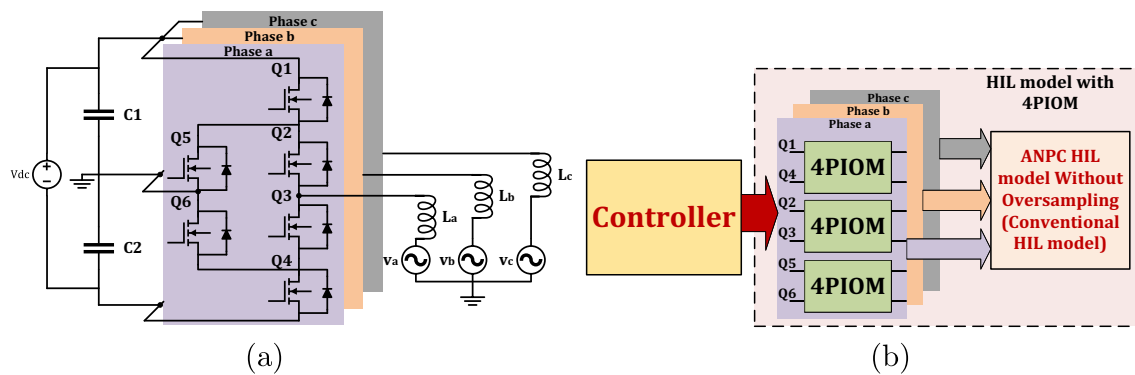


Fig. 9 HIL simulation block diagram for a three-phase ANPC converter; **a** The schematic of the converter connected to the grid **b** Incorporation of 4PIOM blocks in the HIL model

quency and the simulation step of the HIL model (T_{ss}). If T_{ss} is significantly smaller than the switching period of the controller (at least 100 times), oversampling techniques may not be necessary. In such cases, oversampling is only recommended for scenarios where dead time is a critical factor, such as dead time effects analysis [22]. When oversampling is required, the input gate sampling period (T_{is}) must be sufficiently small (smaller than the dead time if the simulation focuses on it), regardless of the selected oversampling method, to accurately capture switching events. The FPGA implementation of oversampling methods enables the reduction in T_{is} down to a few nanoseconds, specifically achieving 5 ns in this study for IOM/4PIOM. Therefore, IOM/4PIOM provide a straightforward solution by maintaining the structure of HIL models without changes. It is important to note that for HIL models involving converters with complementary switches, a hybrid approach utilizing both IOM and 4PIOM is recommended, with the latter exclusively applied to each pair of complementary switches. Another efficient solution involves traditional oversampling methods, which are not affected by the extra delay introduced by IOM/4PIOM. However, the implementation of these methods is more complex and requires additional resources.

6 Conclusion

In this paper, an adaptation of the integration oversampling method (IOM) has been proposed for the HIL simulation of power converters with complementary switches. When IOM is applied to a pair of complementary switches, it may result in a short-circuit problem in the HIL model that introduces offset errors and significant oscillations, as identified by this study. The proposed method (4PIOM) effectively resolves these challenges by applying it to each pair of complementary signals. It reads the complementary signals with a high resolution of 5 ns and generates the switching state with the larger integrated error in each simulation step. For a general

topology with both individual and complementary switches, one IOM block must be applied to each individual switch and a 4PIOM to each pair of complementary switches. These blocks are easy to integrate into complex pre-designed HIL models (e.g., power converter models with many switches) because they are placed outside the model, unlike other classical oversampling methods. Furthermore, they are easy to implement into FPGAs due to the simplicity of the algorithm. However, IOM/4PIOM introduce a slight additional delay caused by the process required to provide the appropriate switching pulses for the HIL model. This limitation is outweighed due to the similarity of their results compared to an ideal oversampling method. Simulation/experimental results of applying 4PIOM to a synchronous buck converter, provided in this paper, show a significant enhancement to the HIL simulation by attenuating the aliasing oscillations and avoiding undesired short circuits that may happen using IOM. 4PIOM reduces the steady-state peak-to-peak aliasing oscillations up to 96% and 94% with respect to the model without oversampling and IOM, respectively. Future research will explore applying this method to more complex topologies, like multilevel converters.

Author Contributions Conceptualization was done by EZ, AS, and AC; methodology was done by EZ and AC; software was done by EZ and AS; validation was done by EZ, AS, and AC; formal analysis was done by EZ and AC; investigation was done by EZ and AS; resources were done by EZ and AC; writing—original draft preparation was done by EZ; writing—review and editing was done by EZ, AS, and AC; visualization was done by EZ and AS; supervision was done by AC.

Funding Open Access funding provided thanks to the CRUE-CSIC agreement with Springer Nature.

Data availability Not applicable.

Code availability Not applicable.

Declarations

Conflict of interest The authors declare that they have no competing interests regarding the publication of this manuscript.

Ethical approval This study was conducted in accordance with ethical guidelines and principles. We confirm that this work is original and has not been published elsewhere, nor is it currently under consideration for publication elsewhere.

Consent to participate All participants included in this study provided informed consent prior to their involvement.

Consent for publication All authors of this manuscript have provided their consent for publication.

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