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High-resolution error compensation in continuous conduction mode power factor correction stage without current sensor

Victor M. Lopez-Martin[1], Francisco J. Azcondo[1], Angel de Castro[2]

[1]University of Cantabria, Santander, Spain, {lopezvm, azcondof}@unican.es
[2]Universidad Autonoma de Madrid, Madrid, Spain, angel.decastro@uam.es

***Abstract* — Continuous conduction mode power factor correction (PFC) without input current measurement is a step forward with respect to previously proposed PFC digital controllers. Inductance volt-second (vs_L) measurement in each switching period enables the estimation of input current, but an accurate compensation of the small errors in the measured vs_L is required. Otherwise, they are accumulated over a half-cycle line, leading to an appreciable current distortion. A vs_L estimation is proposed, measuring the input (v_{in}) and the the output voltage (v_o). Discontinuous conduction mode (DCM) occurs near input line zero crossings, and is detected by measuring MOSFET v_{ds} too. This article analyzes the current estimation error caused by errors in the on-time estimation and voltage measurements, and proposes the minimization of vs_L errors by cancelling the difference between estimated DCM (T_{DCM}^{inreb}) and real DCM (T_{DCM}^{in}) times with a signal (v_{dig}), generated in the digital device. Therefore, the current estimation is calibrated using digital signals during the operation in DCM. Feedfoward coarse time error compensation is carried out with the measured delay of the drive signal, and then a fine compensation is achieved with a feedback loop that adjusts v_{dig}. Experimental results are shown for a 1 kW boost PFC converter.**

***Keywords* —Digital control, power factor correction, sensorless control, digital error compensation, feedfoward control, feedback control.**

I. INTRODUCTION

Some advantages that motivate the use of digital control in PFC stages include: reduction of discrete components, reduction of size, reduction of sensitivity to parameter tolerances, ease of controller implementation and extension of its performance limits. For this reason, current sampling in high-frequency Switched-Mode Power Supplies (SMPS) is an issue in which many authors often pay attention. A resistive sensor is the common adopted solution for current sampling. This resistor causes power losses and a hot spot in the converter. The resistance is defined according with the reference voltage, sensitivity and noise immunity of the circuitry which operates with the sensed current [1]. With regard the analog to digital converter (ADC) speed, the ADC that samples the current must have much higher bandwidth than the voltage ADCs. Different current estimation techniques based in voltage measurements are presented in [2-4] and in [5] for multiphase converter applications. For PFC application, approaches like [6-13] eliminate some of the traditionally required analog to digital conversions.

Similar to [14], DCM operation is used; near input line zero crossings, to correct vs_L estimation in PFC stages without measuring the input current (i_{in}).

The proposed controller avoids the need of current sensing which affect the PFC capabilities (power losses, noise, etc.). It is based on previous works [6, 7] where an input current (i_{in}) estimator removes the current sensor and ADC. With this solution, the PFC designer does not have to pay attention to the current sensor and the controller design.

This paper is organized as follows. A brief overview of the input current estimation without current sensor and the accumulated vs_L estimation error due to drive's signals delays and differences between the estimated inductance and the real one are described in section II. Section III shows estimation errors due to errors in data capture voltage which are due to tolerances and offsets in the voltage measurement circuits (resistors, ADC, etc.), and the resolution of vs_L estimation. A digital compensation of these errors is described in section IV supported with simulation results. Experimental results are presented in section V. Conclusions are given in section VI.

II. CURRENT ESTIMATION WITHOUT CURRENT SENSOR

The digitally input current rebuilding (i_{inreb}) concept, based on input and output voltage measurement, was presented in [6]. Equations (1) and (2) represent the boost converter input current finite difference equations during ON and OFF time respectively, where v_{in}^{adc} and v_o^{adc} are the input and output voltage digital value, respectively. T_{clk} is the clock period and L is the inductor value. The symbol k represents the present clock period.

$$i_{inreb}[k+1] = i_{inreb}[k] + \frac{v_{in}^{adc}[k]}{L} T_{clk} \quad (1)$$

$$i_{inreb}[k+1] = i_{inreb}[k] + \frac{v_{in}^{adc}[k] - v_o^{adc}[k]}{L} T_{clk} \quad (2)$$

The estimated current i_{inreb}, is processed by a digital version of the peak non-lineal carrier (NLC) control described in [15]. As is shown in Fig. 1, i_{inreb} corresponds with the real input current i_{in} under ideal conditions. The duty cycle in each switching period j is represented by $d[j]$, $v_m[k]$ is the value of the carrier signal. The drive signal *on/off* is generated with a switching period T_{sw}.

Since the system is not ideal, there are errors in the inductance volt-seconds (vs_L) estimations due to: 1) the drive signal's delays, 2) the difference between the estimated inductance value and the real one and 3) voltage data errors due to the tolerances of the voltage

dividers and quantization process. Those errors are accumulated over the half-line cycle. The effect of the drive signal's delays is theoretically analyzed in the Appendix I of [6], where it is demonstrated that the most critical error is due to the difference between the ON-to-OFF ($\Delta t_{on\text{-}off}$) delay and the OFF-to-ON delay ($\Delta t_{off\text{-}on}$), which causes the ON-time modification in each switching period defined as $\Delta t_{on} = \Delta t_{on\text{-}off} - \Delta t_{off\text{-}on}$. A positive value of Δt_{on} represents a effective duty-cycle applied to the real input current higher than the one used to estimate the input current, and vice-versa.

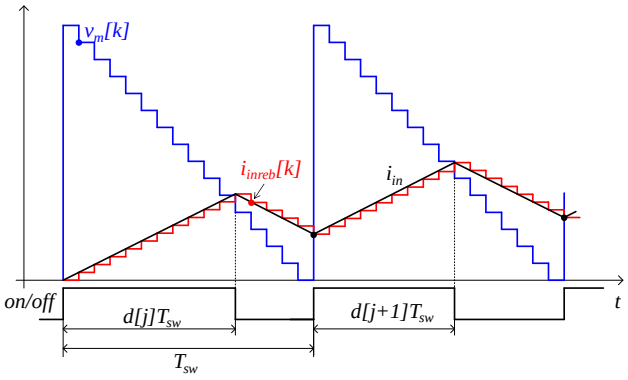


Fig. 1. Digital signals $v_m[k]$ and $i_{inreb}[k]$ compared with the analog real input current i_{in} in ideal conditions.

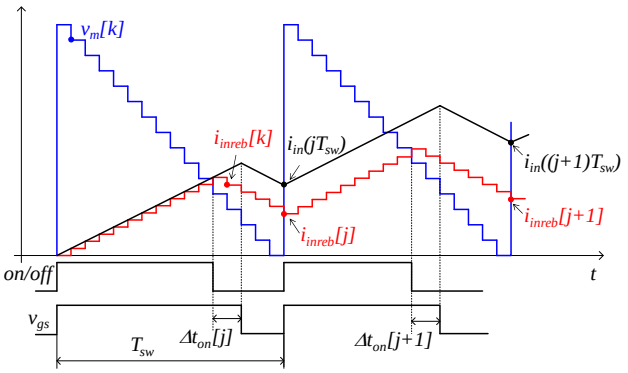


Fig. 2. Digital signals $v_m[k]$ and $i_{inreb}[k]$ compared with the analog real input current i_{in} with drive signal's delays. The *on/off* signal is the output of the digital device, and v_{gs} the MOSFET gate to source voltage.

According to Fig. 2, a current estimation error is defined for a switching period j as $i_{in}^{error}[j] = i_{in}(jT_{sw}) - i_{inreb}[j]$. The error $i_{in}^{error}[j]$ accumulated in n switching periods ($i_{in}^{error}[n]$) is given by (3):

$$i_{in}^{error}[n] = \sum_{j=1}^{j=n} \frac{v_o[j]}{L} \Delta t_{on}[j] \qquad (3)$$

Assuming continuous conduction mode operation, the accumulated current error is $i_{in}^{error}[n_u]$ at the end of the half-line cycle (T_u), being n_u the parameter that represents the total number of switching periods over T_u ($n_u = T_u/T_{sw}$),

$$i_{in}^{error}[n_u] = \frac{V_o}{L} \frac{T_u}{T_{sw}} \Delta t_{on} \quad , \qquad (4)$$

considering a constant output voltage V_o, and a constant ON-time error Δt_{on} over T_u. This accumulated current error does not depend on the load.

A circuit that measures the drive signal's delays followed by a coarse compensation of the NLC algorithm is presented in [7]. The time resolution of the measurement of these delays depends on clock period (T_{clk}) of the digital device.

In the case of ideal PFC operation in CCM, i.e. with the current estimation error totally compensated, a difference between the estimated inductance value (L_{est}) and the real one (L) would result in a difference between the estimated current ripple and the real one, not causing distortion in the average current over a switching period because the L factor affects equally to equations (1) and (2) as it is shown in Fig. 3. Although the ratio given by (5), $i_{inreb}/i_{in} \neq 1$, it is constant over a half utility period (T_u).

$$i_{inreb}[j] = i_{in} \frac{L}{L_{est}} \quad . \qquad (5)$$

The PFC output voltage loop guarantees the desired output voltage (v_o) and correct the estimation error caused by the difference between L and L_{est}.

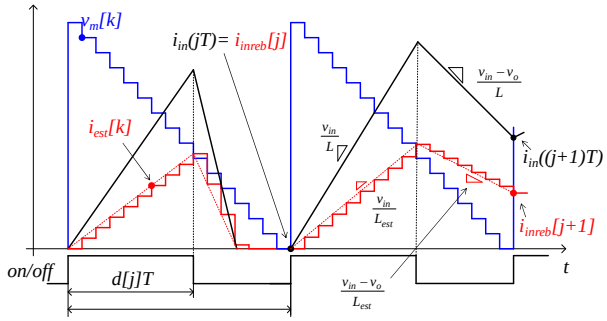


Fig. 3. Digital signals $v_m[k]$ and $i_{inreb}[k]$ compared with the analog real input current i_{in} when the estimated inductance (L_{est}) and the real inductance (L) are different. *on/off* signal is the output signal of the digital device.

III. Errors in Data Capture of Voltage Across the Inductor

Input and output voltage data have a LSB resolution (in Volts) represented by q_{in}^{adc} and q_o^{adc}, respectively, given by (6). The condition to guarantee no distortion in the input current averaged over the switching period $\langle i_{in} \rangle_{Tsw}$, is (7),

$$q_{in}^{adc} = \frac{v_{in}}{v_{in}^{adc}}; \qquad q_o^{adc} = \frac{v_o}{v_o^{adc}} \qquad (6)$$

$$q_{in}^{adc} = q_o^{adc} = \frac{v_{in}}{v_{in}^{adc}} = \frac{v_o}{v_o^{adc}} \quad , \qquad (7)$$

neglecting ADC errors caused by conversion offset and non-linearity.

The current estimation accumulates an error over the half utility period (T_u) if (7) is not fulfilled, resulting in input current distortion. Therefore a current estimation error is generated each switching period because 1 LSB does not represent the same voltage for the input and output voltages.

A difference between q_{in}^{adc} and q_o^{adc} is caused due to errors in the ADCs, tolerances in the resistor divider used to sample the input and output voltage, noise, ADC offsets, etc. Taken the output voltage bin (q_o^{adc}) as reference, the error in the input voltage data (v_{in}^{adc}) expressed in volts, is given by $v_{in}^{error} = v_{in} - v_{in}^{adc} q_o^{adc}$. While condition (7) is not fulfilled, there is a current estimation error each switching period j ($i_{in}^{error}[j]$) depicted in Fig. 4. The parameter n_u represents the total number of switching periods over T_u ($n_u = T_u/T_{sw}$)

$$i_{in}^{error}[n] = \sum_{j=1}^{j=n} \frac{v_{in}^{error}[j]}{L f_{sw}} \qquad (8)$$

On the other hand, the same analysis is performed if the output voltage bin (q_{in}^{adc}) is taken as reference and defining the error in the output voltage data (v_o^{adc}) as $v_o^{error} = v_o - v_o^{adc} q_{in}^{adc}$, the value of the current error accumulated in n switching periods is given by:

$$i_{in}^{error}[n] = -\sum_{j=1}^{j=n} \frac{v_o^{error}[j]}{L f_{sw}} (1 - d[j]) \qquad (9)$$

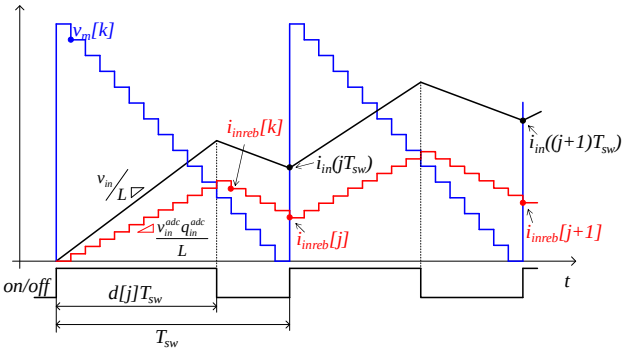


Fig. 4. Digital signals $v_m[k]$ and $i_{inreb}[k]$ compared with the analog real input current i_{in} under errors in data capture of voltage across the inductor. *on/off* signal is the output signal of the digital device.

In order to quantize the current error value, Table I shows the dependence of the current error at the end of the half-line cycle, $i_{in}^{error}[n_u]$, for the two possibilities. At first, with a peak error in the input voltage data $\hat{V}_{in}^{error} = \pm 1$LSB when the output voltage bin value (q_o^{adc}) is taken as reference. The second possibility is for a constant error in the output voltage data $v_o^{error} = \pm 1$LSB taken as reference q_{in}^{adc}. The values presented in the Table I are obtained with (8) and (9) for a in a boost converter whose parameters are L = 1 mH, V_{in} = 230 V_{RMS} (50 Hz) V_o = 400 V_{dc}, f_{sw} = 70 kHz.

The waveform of this error accumulated in n switching periods ($i_{in}^{error}[n]$), is given by (8) and (9), and it is shown over a half-line cycle (T_u) (blue line) in Fig.5.

TABLE I.

AMPS RESOLUTION OF $i_{in}^{error}[n_u]$

	$i_{in}^{error}[n_u]$	
ADC bits	$\hat{V}_{in}^{error} = \pm 1$ **LSB**	$v_o^{error} = \pm 1$**LSB**
10	±2.94 A	∓2.39 A
11	±1.47 A	∓1.19 A
12	±0.73 A	∓0.60 A
13	±0.36 A	∓0.30 A
14	±0.18 A	∓0.15 A

IV. COMPENSATION OF THE CURRENT ESTIMATION ERRORS

The accumulated current error, generated by the error in data capture of input and output voltages v_{in} and v_o, and expressed by (8) and (9) is similar to the current error waveform due to the drive signal's delays [6, 7] and expressed by (3), i.e. both are volt-second errors. This circuit adapts the drain-to-source voltage with a resistor divider and a signal diode to obtain a digital signal (v_{ds}^{dig}) which indicates the real *on-to-off* and *off-to-on* transitions in the converter (Fig. 6).

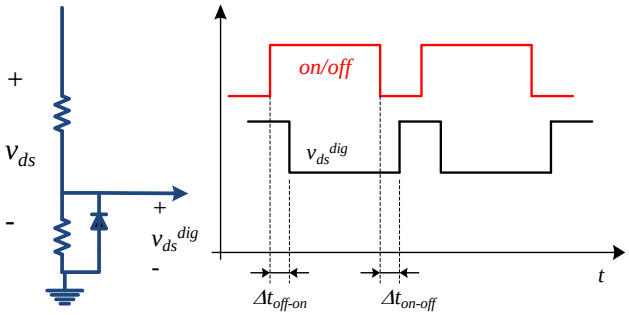


Fig. 6. Auxiliary circuit to adapt the drain-to-source voltage as a digital signal. Comparison with *on/off* signal.

The digital controller compares the *on/off* signal with v_{ds}^{dig} signal to measure the ON-time modification in each switching period (Δt_{on}) and modifies the NLC algorithm

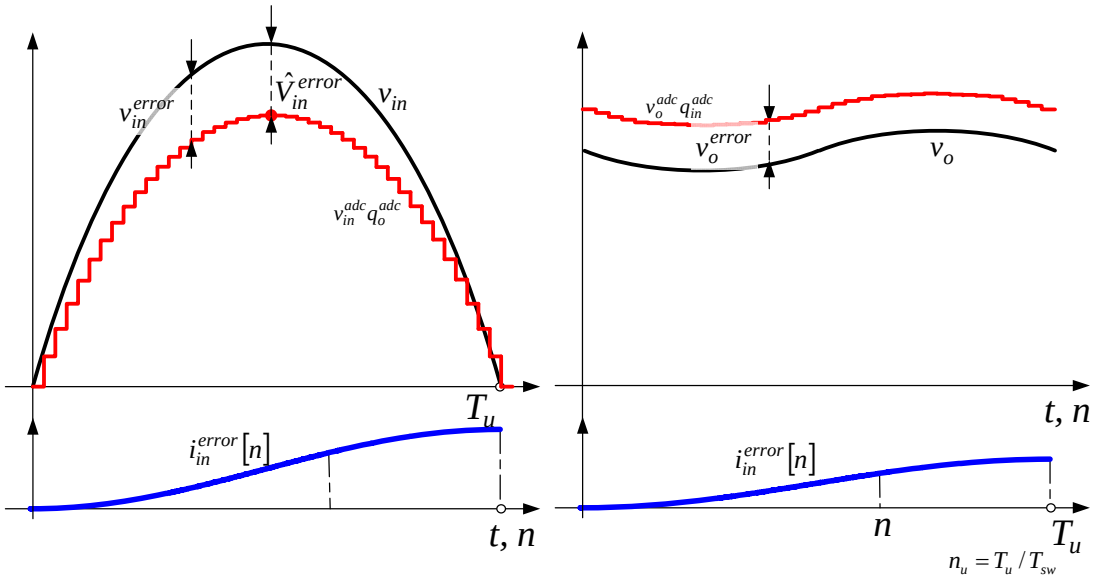


Fig. 5. Accumulated current error in each switching period is represented by $i_{in}^{error}[n]$.Left: Error in the input voltage data. Right: Error in the output voltage data.

as is presented in [7], being a coarse high frequency feedforward compensation of the volt-second errors. The resolution of the Δt_{on} measurement depends on the clock period of the digital device and the minimum error is $\pm T_{clk}/2$. For the Boost parameter values presented before and, a clock period of 10 ns ($\pm T_{clk}/2 = \pm 5$ *ns*) causes a current error at the end of the half line cycle, $i_{in}^{error}[n_u] = \pm 1.40$ A. Selecting $N_{bits} = 14$ bits of resolution in the ADCs, the current error dependence on voltage measurement error is around one order of magnitude more precise than the sensitivity to the drive signal`s delays using a 100 MHz clock frequency.

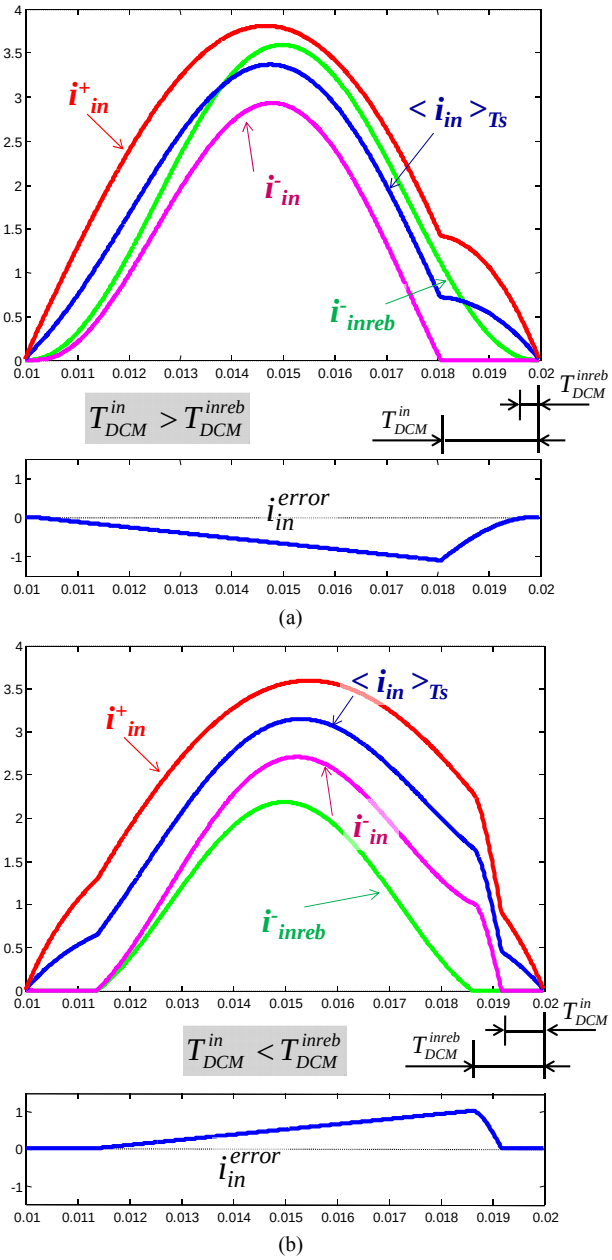


Fig. 7. Simulation results: Difference between estimated DCM time in i_{inreb} (T_{DCM}^{inreb}) and real DCM time in i_{in} (T_{DCM}^{in}) when a drive signal's delay. (a) ΔT_{on} = -5 ns is applied. (b) ΔT_{on} = +5 ns is applied.

Fig 7 shows the current waveforms of the controller assuming the ideal behavior of the ADCs for the input and output voltage measurements, and with a time compensation error of $\pm T_{clk}/2 = \pm 5$ *ns* (highest resolution for the feedforward compensation). The variables i^{+}_{in}, i^{-}_{in}, and $\langle i_{in} \rangle_{Tsw}$ represent the peak, valley and average values of i_{in} in each switching period, respectively; while i^{-}_{inreb} represents the estimated valley input current calculated in each switching period.

Due to the limitation of the compensation resolution and the feedforward nature of the algorithm the zero current estimation error is not assured. A feedback control with fine compensation and higher resolution is applied to fully correct the current estimation error. Using a digital signal v_{dig}, the digital voltage that emulates the output voltage v_o^{adc} is modified, resulting in v_o^{adc*} that is used to rebuilt the input current in equations (1) and (2). The proposed feedback compensator varies v_{dig} injecting a current error compensation with finer resolution than the achieved with the feedfoward time compensation.

$$v_o^{adc*} = v_o^{adc} + v_{dig} \tag{7}$$

This feedback loop is presented in [16] to compensate the parasitic elements effect in the input current estimation. At the same time, the feedback loop corrects estimation errors due to the $\pm T_{clk}/2$ resolution of the Δt_{on} measurement

Discontinuous conduction mode DCM appears near input line zero crossings when the *on/off* signal duty-cycle is limited. The estimated input current i_{inreb}, has an estimated DCM time, defined as (T_{DCM}^{inreb}). Accumulative current error causes a distortion in the input current i_{in}. Therefore, as is shown in Fig. 7, a difference between T_{DCM}^{inreb} and the real DCM time in i_{in} (T_{DCM}^{in}) appears. An auxiliary circuit, is implemented to detect the DCM condition in the real input current i_{in}. This circuit compares the output voltage v_o, with the MOSFET drain-to-source voltage v_{ds}, during OFF time. In CCM operation $v_{ds} = v_o$ during the whole OFF time, but not in DCM. Two digital signals, $DCMi_{in}$ and $DCMi_{inreb}$, are active during the DCM times T_{DCM}^{in} and T_{DCM}^{inreb}, of the real and rebuilt current, respectively.

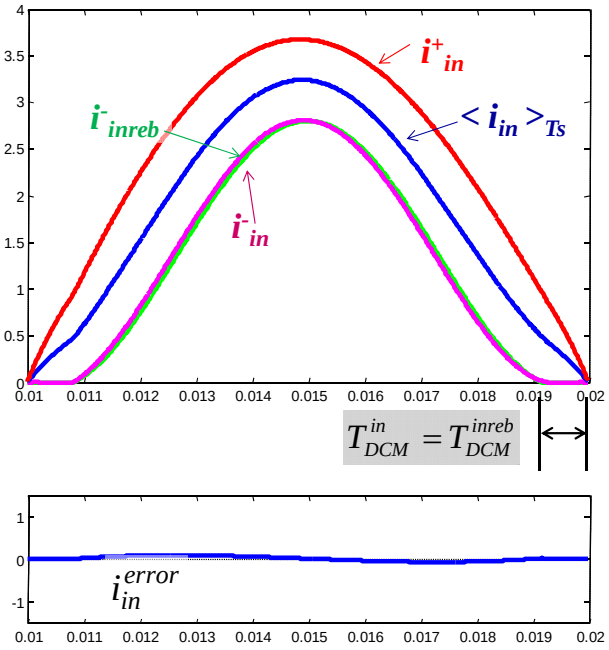
The current estimation error leads to $T_{DCM}^{in} \neq T_{DCM}^{inreb}$ reducing the power factor value. The i_{inreb} controller captures $DCMi_{in}$ and $DCMi_{inreb}$ and, measures and compares T_{DCM}^{in} and T_{DCM}^{inreb}. A time error T_{DCM}^{error}, is expressed in equation (8).

$$T_{DCM}^{error} = T_{DCM}^{inreb} - T_{DCM}^{in} \tag{8}$$

So an indirect measurement of the current estimation error is obtained by measuring the difference between T_{DCM}^{in} and T_{DCM}^{inreb}. If $T_{DCM}^{error} < 0$ (Fig. 7a), then $i_{inreb} > i_{in}$, and it is necessary to decrease the value of v_{dig}. With this, a current compensation error i_{in}^{error} positive (Fig. 5) is injected and i_{in} increases its value. On the other hand, if $T_{DCM}^{error} > 0$ (Fig. 7b), then $i_{inreb} < i_{in}$, and it is necessary to increase the value of v_{dig} in order to inject current compensation error i_{in}^{error} negative. When $T_{DCM}^{error} = 0$, the current estimation error is compensated and as a result of it, the current distortion is minimized.

Fig. 8 shows the PFC waveforms with a correct current estimation for a boost converter with L = 1 mH, V_{in} = 230 V_{RMS} (50 Hz) V_o = 400 V_{dc}, f_{sw} = 70 kHz and output power of 480 W. The time compensation error is Δt_{on} = +

5 ns and the feedback loop sets v_{dig} = *8 LSB* (q_{in}^{adc} = *0.0289 V/bit*). In this situation, there is no difference between estimated DCM time in i_{inreb} (T_{DCM}^{inreb}) and real DCM time in i_{in} (T_{DCM}^{in}).



(a)

Fig. 8. Simulation results: DCM time in i_{inreb} (T_{DCM}^{inreb}) and real DCM time in i_{in} (T_{DCM}^{in}) are matched when Δt_{on} = + 5 ns and the feedback loop sets v_{dig} = *8 LSB* (q_{in}^{adc} = *0.0289 V/bit*).

V. Experimental Results

Laboratory experiments that illustrate the behavior of the auxiliary circuit that captures the drain-to-source voltage and the performance of the error compensation have been carried out with a 1 kW Boost converter. Fig. 9 shows a schematic diagram of the power converter, the digital device and the analog part of the control, whose parameters are presented in Table II. The power stage reactive components are: L = 1 mH, C = 220 µF, and the switching frequency is f_{sw} = 70 kHz. The input voltage is V_{in} = 230 V_{rms} (50 Hz), and the output voltage is V_o = 400 V_{dc}. The MOSFET and diode used to build the power stage were a IRFP27N60K from International Rectifier and a RHRP860 from Fairchild Semiconductor, respectively. A custom inductor of the required value was built using a soft-saturation core, Kool-mµ 77110 to increase the CCM operation for a large load range. A 2nd-order ad-hoc Σ–Δ analog to digital converter as described in [3] and [5] is used to measure the output voltage. For the input voltage a 10 bits TLV1572 commercial ADC from Texas Instruments has been used to minimize nonlinearities in the input voltage data.

Figure 10 shows the waveforms of the auxiliary circuit implemented to adapt v_{ds} as a digital signal. Drain-to-source voltage is a high voltage pulsated waveform with 400 to 0 Vdc and 0 to 400 Vdc steps. The MOSFET parasitic elements cause non ideal transients. The off-to-on transition is presented in Fig. 10a, where the event in v_{ds}^{dig} coincides with the valley value of the real input current (i_{in}). The on-to-off transition is shown in Fig. 10b. In this situation a time delay exists between the v_{ds}^{dig} event and the real transition. This delay causes an additional current distortion that is corrected with the feedback loop.

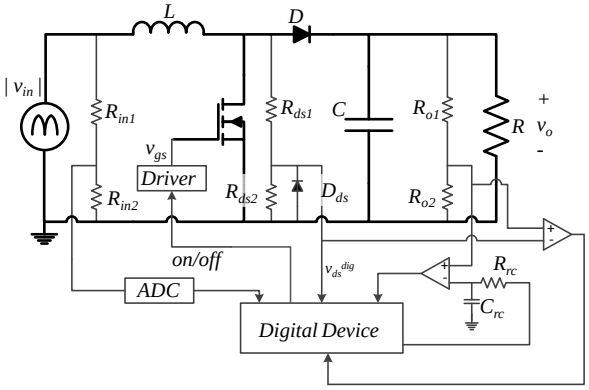
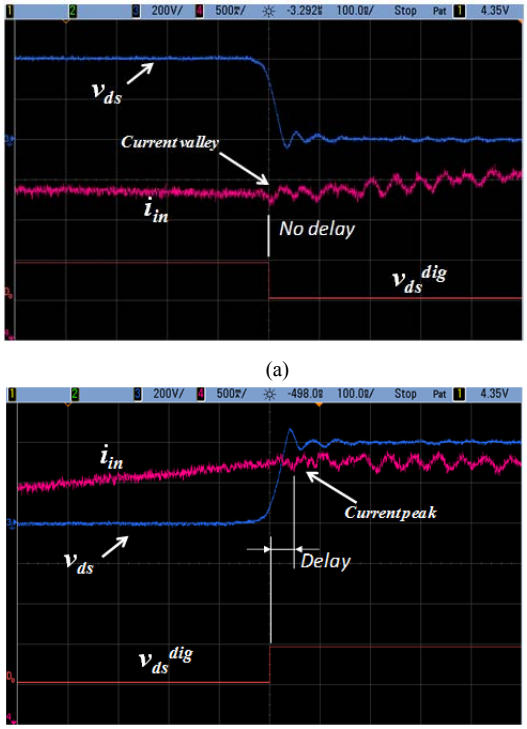


Fig. 9. Schematic diagram of the Boost PFC converter

TABLE II.

CONVERTER CONTROL PARAMETERS

$R_{in1} = R_{o1}$	1 MΩ
$R_{in2} = R_{o2}$	10.7 kΩ
R_{ds1}	1 MΩ
R_{ds2}	10.7 kΩ
D_{ds}	1N4148
R_{rc}	2.2 kΩ
C_{rc}	6.8 nF
Comparators	MAX942
Digital Device	XC3S200E FPGA



(a)

(b)

Fig. 10. Waveforms of the auxiliary circuit implemented to adapt v_{ds} as a digital signal (a) Off-to-on and (b) On-to-off transition.

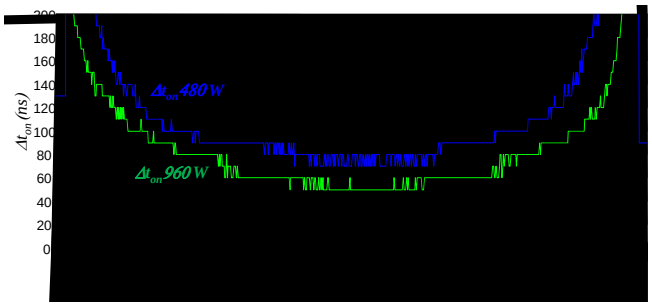


Fig. 11. Value of the duty cycle modification (Δt_{on}) due to drive's signal delays over the half line cycle.

The on-time modification (Δt_{on}) due to drive's signal delays over the half line cycle is shown in Fig. 11 for different loads (480 W and 960 W). These delays are function of the MOSFET gate resistor value, drain current and the MOSFET parasitic elements. With the auxiliary circuit shown in Fig. 6, the value of Δt_{on} is measured each switching period and the NLC algorithm is compensated instantaneously,.

Figure 12 shows the case $T_{DCM}^{error} > 0$, then $i_{inreb} < i_{in}$ while Fig. 13 corresponds to the opposite case $T_{DCM}^{error} < 0$ and $i_{inreb} > i_{in}$,. In both cases the output power is P_o = 480W. In the first case the measured power factor is 0.967, and 0.944 for the second case. It can be observed that the experimental results are in agreement with simulation results presented in Section IV.

Figures 14, 15, and 16 show the steady-state input current, when the feedback control with digital compensation acts and DCM times are matched, under different load conditions (970, 805 and 330 W, respectively). The input current takes a sinusoidal shape when $T_{DCM}^{error} \approx 0$, and the measured power factor and THD of the input current values are presented in Table III.

The time evolution of the T_{DCM}^{error} value under a load step down (970-640 W) is shown in Fig. 15. After the error value peak that occurs when the load step is applied, the fine error feedback loop modifies the v_{dig} amplitude, compensating the T_{DCM}^{in} and T_{DCM}^{inreb} difference reaching a steady state condition with $T_{DCM}^{error} = 0$.

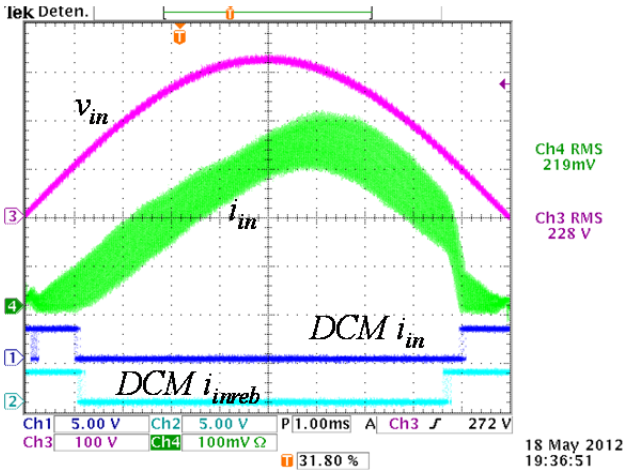


Fig. 12. Experimental results. Input voltage v_{in}, real input current i_{in} waveforms and digital signals $DCMi_{in}$ and $DCMi_{inreb}$ for $T_{DCM}^{error} > 0$, then $i_{inreb} < i_{in}$.

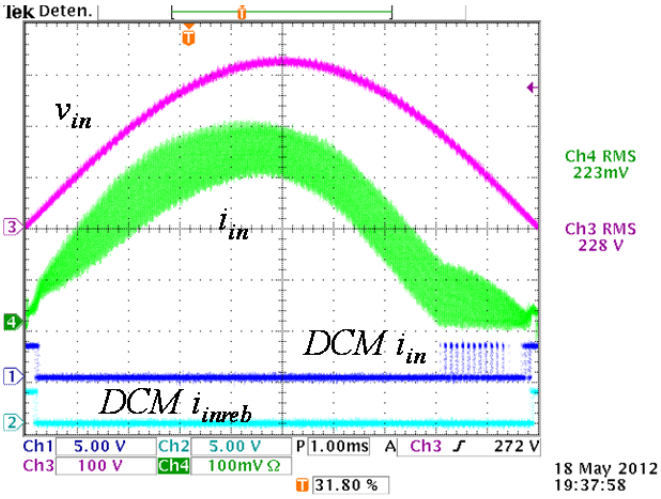


Fig. 13. Experimental results. Input voltage v_{in}, real input current i_{in} waveforms and digital signals $DCMi_{in}$ and $DCMi_{inreb}$ for $T_{DCM}^{error} < 0$, then $i_{inreb} > i_{in}$

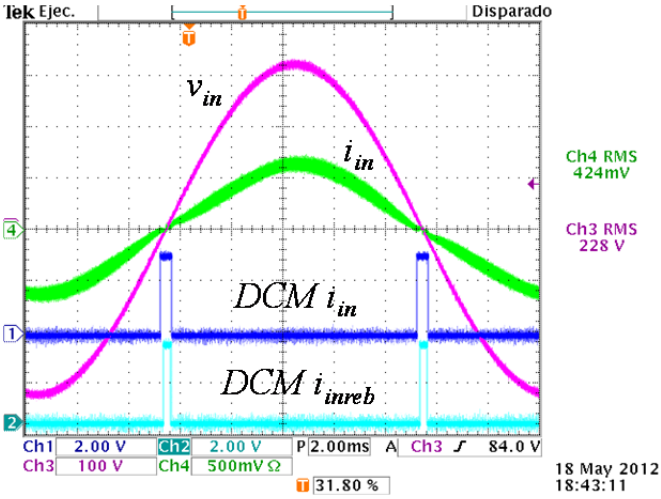


Fig. 14. Experimental results (970 W). Input voltage v_{in}, real input current i_{in} waveforms and digital signals $DCMi_{in}$ and $DCMi_{inreb}$ for $T_{DCM}^{error} \approx 0$, then $i_{inreb} \approx i_{in}$

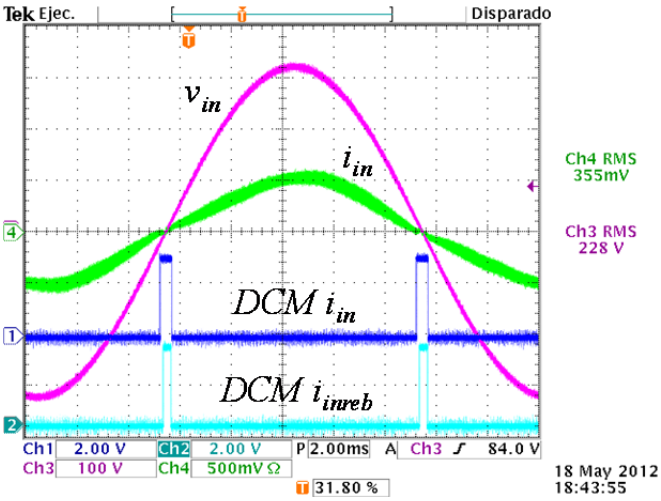


Fig. 15. Experimental results (805 W). Input voltage v_{in}, real input current i_{in} waveforms and digital signals $DCMi_{in}$ and $DCMi_{inreb}$ for $T_{DCM}^{error} \approx 0$, then $i_{inreb} \approx i_{in}$

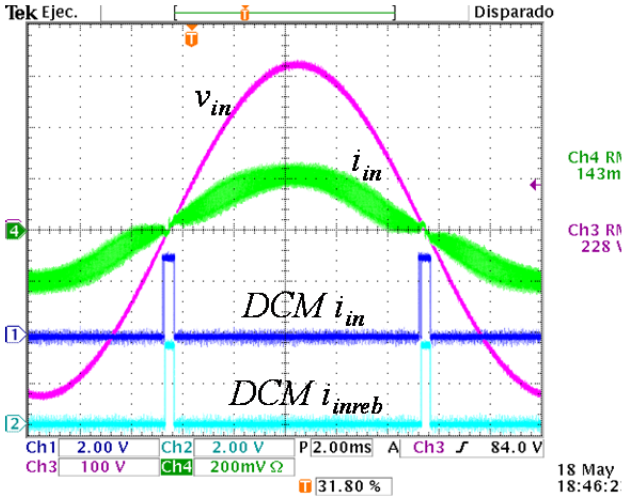


Fig. 16. Experimental results (323 W). Input voltage v_{in}, real input current i_{in} waveforms and digital signals $DCMi_{in}$ and $DCMi_{inreb}$ for $T_{DCM}^{error} \approx 0$, then $i_{inreb} \approx i_{in}$

TABLE III.

EXPERIMENTAL RESULTS: OUTPUT POWER, POWER FACTOR AND THD OF THE INPUT CURRENT FOR DIFFERENT LOAD CONDITIONS. EUROPEAN GRID

Input Voltage	Output Voltage	Input Power	Power Factor	THDi
230 V_{RMS}	400 Vdc	970 W	0.998	6.5 %
		805 W	0.997	6.4 %
		643 W	0.996	8.0 %
		480 W	0.995	9.0 %
		323 W	0.991	10.1 %

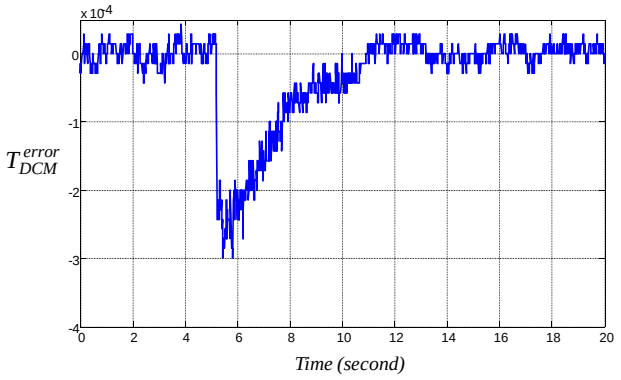


Fig. 17. Experimental results. $T_{DCM}^{error} = 0$ time evolution under a 970 to 640 W load step down.

VI. CONCLUSIONS

An universal current sensorless controller for Boost PFC stages operating in CCM has been presented.

Uncompensated drive signal's delays as small as 5 ns (minimum time compensation error) and voltage acquisition errors, accumulated over half the utility period, distort the input current and reduce the power factor value.

The effects of the drive signal delays and input and output voltage measurement errors in the input current estimation have been analyzed and compensated by the combination of feedforward and feedback strategies that modify the MOSFET on time and the acquired output voltage respectively. A single digital signal acquired from the MOSFET drain-to-source voltage drop is used by both feedforward and feedback compensators.

The error between the estimated and actual DCM intervals close to the zero crossing of the input voltage is a key variable in the feedback strategy to accurately correct the error in the estimation of the input current and the consequent distortion.

The feedback compensation successfully generates a digital signal that provides the acquired output voltage with a resolution as fine as required to fully compensate the inductor volt-second estimation error. Experimental results show a boost PFC converter under different load conditions achieving high power factor with a reliable performance.

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