Single ADC Single Loop Power Factor Correction using Pre-Calculated Duty Cycles

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Keywords

<<Regulation>>,<<Power factor correction>>, <<Switched-mode power supply>>,<<Field Programmable Gate Array (FPGA)>>.

Abstract

PFC controllers usually need three sensors. A digital implementation with pre-calculated duty cycles can reduce the number of sensors. The disadvantage of using pre-calculated duty cycles is that power factor is very sensitive to any non-idealities, so some kind of regulation is necessary. A single ADC and single loop technique is proposed and it obtains a high power factor under non-nominal conditions.

Introduction

Traditional PFC systems sense three parameters: the input and output voltages, and the input current. Every sensor increases the complexity, cost and size of the converter. Especially, the input current sensing is not a trivial issue, because a trade-off between cost, power losses, accuracy and bandwidth must be reached [1, 2]. A common practice is to use a resistive sensor, but the resistor implies power losses and the generated heat must be evacuated.
Digital control of PFC converters allows us to reduce the number of sensors of the systems. Several proposals to avoid the current sensing have been introduced in the recent years. One approach is to estimate the input current measuring the input and output voltages of the converter [3, 4]. Other methods ignore the current measuring and they only implement a voltage loop [5].
Another approach to avoid the current sensing is to pre-calculate a set of duty cycles which will be applied to the switch of the converter. This is possible because power factor correction is a periodic task. These cycles are applied periodically but they must be synchronized with the ac mains. In [6] a predictive algorithm is presented, which pre-calculates the duty cycles for the next ac period, measuring the input and output voltages of the present period. Therefore, non-negligible calculus is needed to calculate online the duty cycles for the next ac semiperiod.
Another approximation is to calculate the duty cycles offline in a computer, with all the desired accuracy, even modeling the non-idealities of the converter. In this way, only a memory, an ac mains zero-crossing detector and a simple controller are used to apply these values. The set of duty cycles are calculated for nominal conditions and must be modified in case of different working conditions. In [7] several sets of duty cycles are calculated and only one is applied depending of the operation conditions. As the number of sets that can be stored is limited, the system gets undesirable results if no set of duty cycles fits with the real conditions.
This proposal presents a method to control a simple PFC converter with pre-calculated duty cycles. Only one set of pre-calculated duty cycles is read from a memory, and a voltage loop controls the output voltage of the converter. Different regulation approaches are explained and compared.

Implementation

Pre-calculation

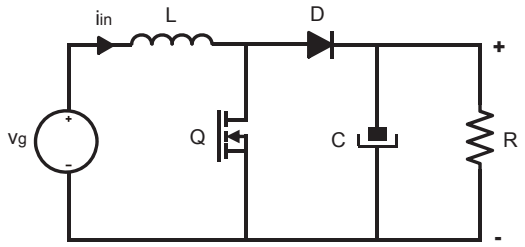


Figure 1: Model of a boost converter

The duty cycles set can be pre-calculated offline and accurately with a computer. The calculation varies depending on the topology, and a boost converter (see Fig. 1) is used in this paper. However, the calculus for other topologies is analogous. In the case of a boost converter working in CCM, the duty cycle of the switching period k is:

$$d(k) = \frac{v_{out}(k) - v_g(k)}{v_{out}(k)} + \frac{L}{T_{Sw}} \cdot \frac{(i_{in}(k+1) - i_{in}(k))}{v_{out}(k)} \tag{1}$$

where d is the duty cycle, L is the inductance of the coil, v_g is the input voltage and v_{out} is the output voltage. Eq. (1) does not take into account the power losses of the converter. As it was explained before, these non-idealities components can be added, but they have been omitted in this paper for the sake of clarity.
Once a set of duty cycles is pre-calculated and stored in a memory, the system has to synchronize the memory with the ac mains. This can done by measuring the input voltage with an ADC, or using a voltage comparator in order to detect the zero-crossing, which is less expensive and less complex. Moreover, it is important to notice that this comparator can have low bandwidth, because the rectified input voltage has a frequency of 100 or 120 Hz.
If the working conditions, such as input voltage, output load, or non-idealities are different from expected, the output voltage will differ from its nominal value. Therefore, it is always necessary to include a compensator to modify the stored duty cycles. The proposed system in this paper only measures the output voltage. In order to regulate the output voltage, the following average equation of a boost converter in CCM can be taken into account:

$$< d >_{Tu} = \frac{< v_{out} >_{Tu} - < v_g >_{Tu}}{< v_{out} >_{Tu}} \tag{2}$$

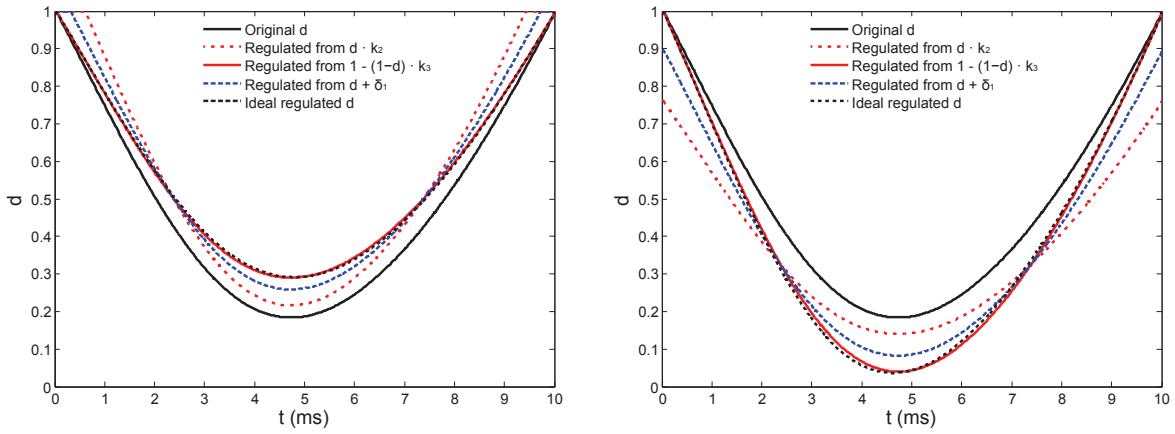
where $< d >_{Tu}$, $< v_{out} >_{Tu}$ and $< v_g >_{Tu}$ are average values during an ac semiperiod, Tu. When the average output voltage during an utility period, $< v_{out} >_{Tu}$, is different from expected, the duty cycle should be changed accordingly. The dynamic of the output voltage is slow, so a simple PID regulator can be used. This compensator is like a classic output voltage loop in a PFC converter, and it updates its output each utility period. However, using the pre-calculation technique, not only one duty cycle must be modified, but a full set of duty cycles should be changed. Next sections show three techniques for regulation of pre-calculated duty cycles.

Regulation method 1

One method is to change every duty cycle adding or subtracting the output of the regulator, which is similar to other typical voltage loops. In this way, the final duty cycle during the switching period k, $d_{f1}(k)$, is:

$$d_{f1}(k) = d_o(k) + \delta_1 \tag{3}$$

where $d_o(k)$ is the pre-calculated duty cycle of the same period, and δ_1 is the output of the regulator, which is constant during the utility period. This regulation is suitable in dc-dc converters, but in ac-dc converters it produces distortions in the duty cycle shape, as it can be seen in Fig. 2.



(a) Regulation +15%. (b) Regulation −15%.

Figure 2: Different regulation methods.

Fig. 2(a) shows the resulting set when the output voltage is 15% lower than expected so the regulation is positive. It shows the original set, the ideal regulation under the new conditions, and the result of this method, and the other two methods that will be presented. Likewise, Fig. 2(b) shows the set after regulation when the output voltage is 15% higher than the nominal value, so negative regulation is applied. Regulation of 15% is not frequent, but it has been shown in order to see clearly the results of the three methods.
The problem that arises with this method is that the duty cycle in power factor correction must start and end at value 1 to achieve high power factor. On the one hand, if δ_1 is lower than 0, the modified duty cycles begin and end under 1. On the other hand, if δ_1 is bigger than 0, this method saturates the duty cycle at 1 during several switching cycles which also worsens the power factor.

Regulation method 2

The second method is to multiply all the duty cycles during a utility period by the output of the compensator, k_2:

$$\begin{aligned} d_{f2}(k) &= d_o(k) \cdot k_2 \\ k_2 &= (1+\delta_2) \end{aligned} \tag{4}$$

In this way, the new set, d_{f2}, is proportional to the original one. The regulator outputs a value of 1 under nominal conditions, and it is modified around this value through changes in δ_2, as seen in Fig. 3. This method also distorts the duty cycle set and, accordingly, the power factor, as seen in Fig. 2.

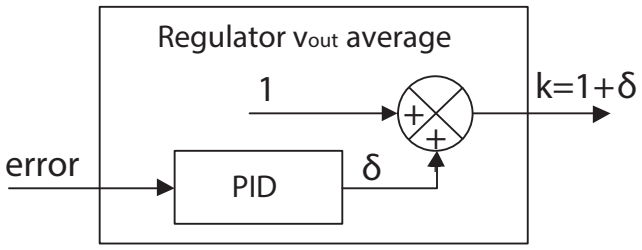


Figure 3: Regulator diagram for method 2 ($d \cdot k_2$) and method 3 ($1-(1-d)\cdot k_3$)

Regulation method 3

The goal is to use a method that barely distorts the duty cycle set when it is regulated, so higher power factor will be reached. The third method stores in memory a set with $(1-d)$ values, instead of d:

$$d_{f3}(k) = 1 - (1 - d_o(k)) \cdot k_3$$
$$k_3 = (1 + \delta_3) \tag{5}$$

Similarly to the previous method, k_3 is the output of the regulator, being 1 under nominal conditions, and being modified around this value through δ_3. When $(1-d)$ is multiplied by the output of the regulator, the duty cycle sequence keeps the initial and final shape. It is because the initial and final values of the duty cycles set, which are saturated to 1, are converted to 0 due to the $(1-d)$ transformation, so any multiplication does not modify the shape when the transformation is undone. In this way, this method modulates the difference between the duty cycles and the value 0. The modified duty cycle set using this method will be very similar to the ideal regulation.
The loop used in the method $1-(1-d)\cdot k_3$ is shown in Fig. 4. The output of the regulator k, equivalent to k_3 in Eq. (5), multiplies the complementary duty cycle $(1-d)$, obtaining the regulated complementary duty cycle $(1-d)^*$. Finally, this complementary duty cycle is translated into actual duty cycle, d^*, equivalent to d_{f3} in Eq. (5).

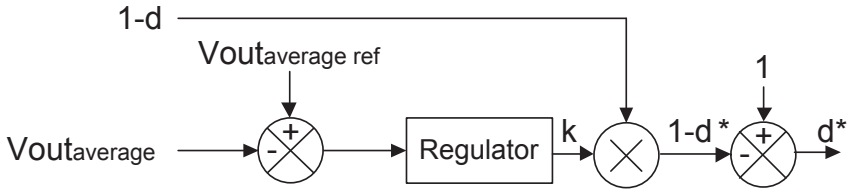


Figure 4: Loop for $1-(1-d)\cdot k_3$ method

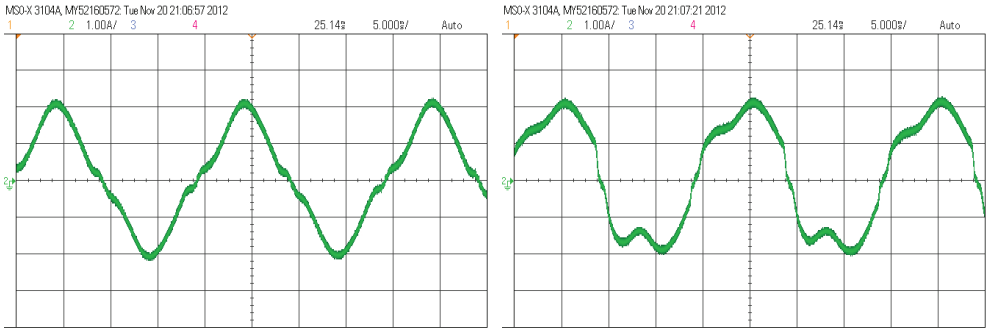
The regulator is similar to the one used in the second method (see Fig. 3). The controller is based on a PID regulator with output δ, which is added to 1. Therefore, the final output is $1+\delta$, where δ is equal to 0 and k equal to 1 in nominal conditions. However, the output is increased or decreased around 1 to control the output voltage.

Results

Table I: Converter Parameters used for testing

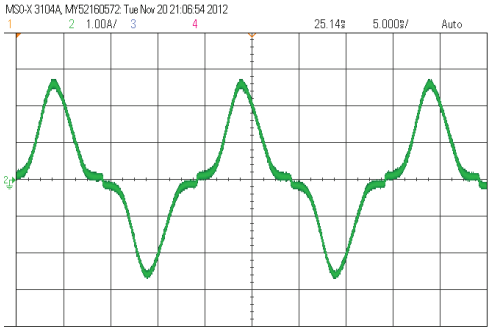
Parameter	V_g	V_{out}	P	C	L	F_{Sw}
Value	230 V	400 V	5 mH	68 μF	100 kHz	

All the methods proposed in the previous section have been tested with a real converter. The boost converter which has been used has the parameters described in table I. The controller (including the compensator, duty cycles memory and synchronization) has been implemented inside an FPGA Xilinx XC3S1000-4FT256. The switching frequency is 100 kHz, using a PWM with 1 000 possible values. Finally, the utility period has been divided into 1 000 switching cycles.
The pre-calculated duty cycles (d for methods 1 and 2, and $1-d$ for method 3) are stored in the block RAMS of the FPGA. Every duty cycle is stored with 16 bits, using 11 to store a value between 0 and 999, and 5 to store fractional bits of the duty cycle. These fractional bits are used to implement a dither technique [8], to increment the resolution of the PWM signal. Taking all into account, the whole set of duty cycles are stored in 16 000 bits, so only one block RAM can be used as the block RAM capacity is 16 kb.
The voltage loop only uses one ADC to measure the output voltage in several points during an utility period. The FPGA calculates the mean value of the output voltage, and the difference between the voltage reference and the actual mean value is the input of the voltage loop.
The synchronization with the ac mains has been implemented with a voltage comparator which detects the zero-crossing of the rectified input voltage. A simple digital filter has been implemented to reduce the noise of the analog comparator and it generates only one pulse when the memory addressing must be reset.
All the results have been acquired using an oscilloscope Agilent MSO-X-2104-A, while the input current has been sensed using a current probe Agilent 1147A. The harmonic distortion of the input current and the power factor has been calculated using the FFT of the oscilloscope, processing the even harmonics (first to thirteenth) of the input current.
The experiments have tested the three methods under regulations of -4% and $+4\%$, which is less regulation than Figs. 2(a) and 2(b), but it is more realistic.

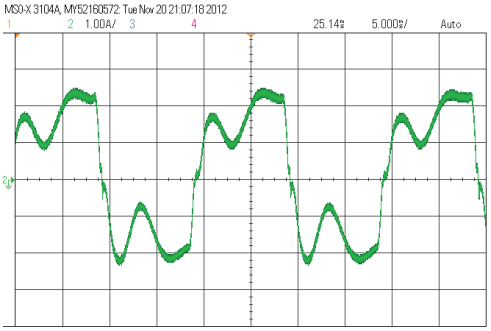


(a) $d+\delta_1$ method. Regulation -4%.

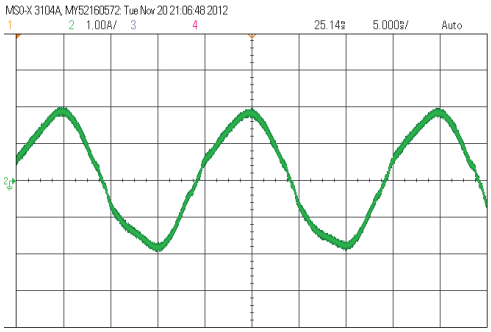
(b) $d+\delta_1$ method. Regulation $+4\%$.



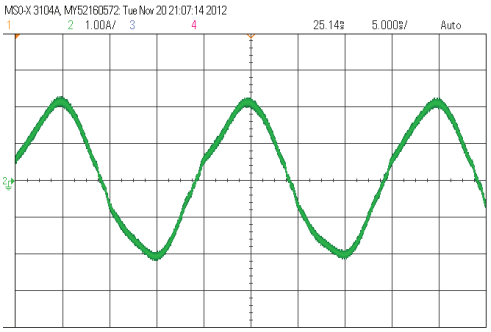
(c) $d \cdot k_2$ method. Regulation -4%.



(d) $d \cdot k_2$ method. Regulation $+4\%$.



(e) $1-(1-d)\cdot k_3$ method. Regulation -4%.



(f) $1-(1-d)\cdot k_3$ method. Regulation $+4\%$.

Figure 5: Input current with non-nominal output voltage.

Fig. 5 shows that the method $1-(1-d)\cdot k_3$ achieves high power factors under non-nominal conditions. Method $d+\delta_1$ gets worse results, especially under positive regulation. Finally, method $D \cdot K_2$ gets the worst results, which are not acceptable in PFC.
Table II shows the power factor and input current harmonic distortion (input current THD). The results of the table shows clearly the improvement achieved using the third method, obtaining power factors around 0.99 in both cases.

Table II: Power factor and harmonic distortion with non-nominal output voltage

	Regulation $+4\%$		Regulation -4%	
	PF	**THDi**	**PF**	**THDi**
$D+\delta$ method:	0.97287	16.6994%	0.95655	21.31376%
$D \cdot K_2$ method:	0.87327	38.09488%	0.77220	54.31353%
$1-(1-d)\cdot k_3$ method:	0.99465	7.33733%	0.99467	7.32328%

Finally, a harmonic test has been accomplished for the three methods to know if the proposed methods reach the harmonics regulation EN 61000-3-2. Only the odd harmonics have been analyzed, because the even harmonics are very small and the oscilloscope does not have enough resolution to measure them with accuracy. Table III summarize the results of Class C test for the third method, which is the most

restrictive class.

Table III: Class C normative for the three proposed methods

	Normative accomplishment		
Method	Reg. $+4\%$	Nominal	Reg. -4%
1) $d+\delta$:	Yes	Yes	Yes
2) $d \cdot k_2$	No	Yes	No
3) $1-(1-d)\cdot k_3$	Yes	Yes	Yes

As it can be seen, the first and last method pass the normative in all the cases, while the second method does not meet the normative with non-nominal conditions. Table IV shows the results of the test for nominal conditions with the third method $(1-(1-d)\cdot k_3)$.

Table IV: IEC 61000-3-2 class C test for method 3 $(1-(1-d)\cdot k_3)$. Values in amperes.

Harmonic	**Value measured**	**Max. Class A**	**Max. Class B**	**Max. Class C**	**Max. Class D**
1^{st}	1.241				
3^{rd}	0.075	2.300	3.450	0.371	1.020
5^{th}	0.013	1.140	1.710	0.124	0.570
7^{th}	0.011	0.770	1.155	0.087	0.300
9^{th}	0.012	0.400	0.600	0.062	0.150
11^{th}	0.007	0.330	0.495	0.037	0.105
13^{th}	0.002	0.210	0.315	0.037	0.089

Conclusions

Digital control for power converters makes possible to reduce the number of required measures in PFC techniques. This paper proposes a low-cost method to regulate the duty cycles of a PFC converter based on pre-calculation of $(1-d)$. The proposed method only measures the output voltage with an ADC. Besides, synchronization with the ac mains is reached with a low-cost comparator. Results shows that the proposal achieves high power factors even with non-nominal conditions.

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