Pre-Calculated Duty Cycle Control Implemented in FPGA for Power Factor Correction

Alejandro Garcia[1], Angel de Castro[1], Oscar Garcia[2], Francisco J. Azcondo[3]

[1]*HCTLab, Univ. Autónoma de Madrid. Francisco Tomás y Valiente 11, Madrid, Spain*

angel.decastro@uam.es

[2]*CEI, Univ. Politécnica de Madrid. José Gutiérrez Abascal 2, Madrid, Spain*

[3]*TEISA, Univ. De Cantabria. Av. De los Castros s/n, Santander, Spain*

Abstract— **A power factor correction (PFC) technique based on pre-calculated duty cycle values is presented in this paper. In this method the duty ratios for half a line period are calculated in advance and stored in a memory. By synchronizing the memory with the line, near unity power factors can be achieved in a specific operating point. The main advantage of this technique is that neither current measurement nor current loop are needed. To obtain stable output voltages a voltage loop is included. A boost converter prototype controlled by an FPGA evaluation board has been implemented in order to verify the functionality of the proposed method. Both the simulation and experimental results show that near unity power factor can be achieved with this PFC strategy.**

Keywords— **Power Factor Correction, Switched Mode Power Supply, Boost Converter, Field Programmable Gate Array, Digital Control.**

I. INTRODUCTION

In order to comply with the requirements of international standards of harmonics emissions, such as EN16000-1-2, in most ac-to-dc switched mode power supplies (SMPS) the implementation of PFC is necessary. Achieving almost unity power factor, the voltage distortion and losses are reduced, there is no reactive power, and less current is needed, resulting in increased system efficiency and reduced customer's utility bills.

Power factor correction in SMPS has been conventionally performed with analog controllers. The proliferation of powerful and low cost digital devices, such as microprocessors, digital signal processors (DSP) and field programmable gate arrays (FPGA) has made possible to implement digital controllers of SMPS in a competitive way [1-3]. Digital control has many advantages with respect to analog control, such as increased reliability and reproducibility of the systems, more complex algorithms, lower noise sensitivity, and easy signal monitoring.

The control in PFC is typically done with two loops: an internal and fast current loop to achieve near unity power factor, and an external and slow voltage loop to stabilize the output voltage (Fig. 1). In this case, usually three measurements are necessary: input and output voltage (v_{in} and V_{out} respectively), and input current (i_{in}). One of the main advantages of the control technique proposed in this paper is that the measurement of the current, which is a complex and costly process, is not needed.

There have been other previous proposals in which the current is also not measured. In [4-5] a digital off-line control technique called stored-duty-ratio is proposed. In that method, because the predictability and periodicity of duty ratios in PFC, the values of the duty cycle are calculated in advance and stored in an EPROM, so current and input voltage sensing are neither required. The values of the duty cycle stored in the memory are transformed into the control pulse width modulation (PWM) signal by a microcontroller device. The only signals required from the boost converter to the control system are the line synchronization and the output voltage, if output voltage control is performed. Two versions are studied. The first one is an "uncontrolled version", in which there is only one set of duty cycles stored, so power factors near 0.99 can only be achieved in one specific operation point. In the "controlled version" eight different sets of duty ratios are applied on-line depending on the input voltage, so there are eight operating points and near unity power factor can be achieved in a wider range of input voltages. This "controlled version" is implemented using also analog devices.

In [6] a predictive method, similar to the previous one, is presented, in which the duty cycle values are generated in advance in each half line period, but during operation. The control algorithm is based on the input voltage, reference output voltage, inductor current and reference current. Due to the high switching and computation speeds required, the system is based on a high-end DSP device. Since the values are calculated dynamically in each half period, unity power factor can be achieved in a wide range of input voltages and output powers, and also in transient state for step load change and input voltage change. As in the previous method, current sensing is avoided. In [7] a similar method is studied, but the system is implemented in an FPGA.

In [8] a PFC technique based on the digital reconstruction of the input current on a boost converter is presented. In this technique a current loop is implemented, but since the current values are estimated there is no need in measuring current.

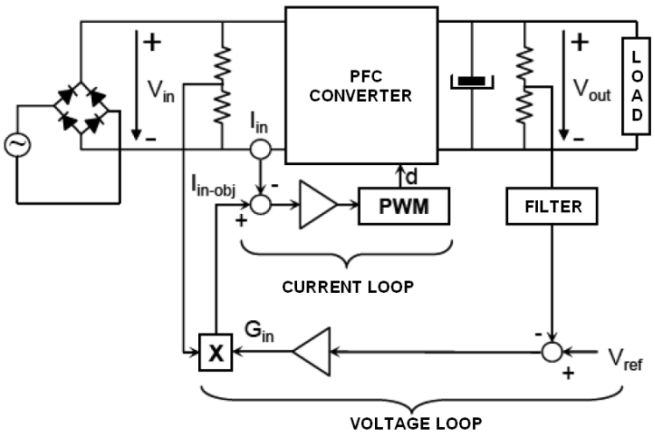

Fig. 1. Typical control in PFC with current and voltage loop

The implemented algorithm, based on the one-cycle-control, estimates the value of the current continuously, so the rebuilding update frequency sets the resolution of the PWM signal and, because of that, a custom hardware implementation, such as FPGA used in that publication, is more appropriate than a microprocessor or DSP implementation. As in the previous publications, the input current does not need to be measured.

Finally, in [9] the current measurement is avoided and a single voltage loop is implemented based on phase-shifting the input voltage measurement. A DSP is used for the implementation, and the resolution of phase-shifting is critical.

In this paper a current sensorless control method of power factor correction for a boost converter based on pre-calculated duty cycle values is proposed, which is similar to the proposal of [4-5]. In this technique, apart from the generation of the PWM signal from stored duty ratios and the synchronization with the rectified input voltage, neither current measurement and current loop nor complex operations or algorithms are needed. The main difference with the proposal of [4-5] is that a voltage loop is included, but using a single set of pre-calculated duty cycle values. Furthermore, only a digital device (FPGA) is used in the controller. Apart from that, an exhaustive study of the effects of different design parameters (such as the inductor and capacitor values or the mismatch in the synchronization) is included. Since the duty cycle values are calculated off-line, near unity power factors can only be achieved in nominal conditions. The rest of the paper is organized as follows. In Section II the pre-calculated duty ratios method is studied. Simulations of the effect of different parameters are included. In Section III the voltage loop and his effect on the resultant power factor is presented. The hardware implementation and experimental results are presented in Section IV. Finally, conclusions are presented in Section V.

II. PRE-CALCULATED DUTY CYCLE VALUES

The proposed control system is based on calculating off-line the duty cycle values needed for PFC for specific conditions of input voltage and output power in a boost converter. The topology of the boost converter is shown in Fig. 2. Actually, there are two components of the duty cycle (see Fig. 3):

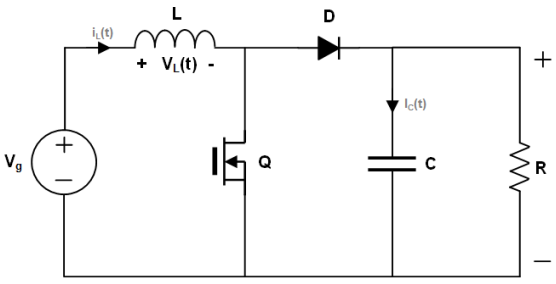

Fig. 2. Boost converter topology.

$$d(k) = d_1(k) + d_2(k) \tag{1}$$

The first component sets the relationship between the input and output voltages, which can be obtained from the volt·second balance in the inductor. Because the switching frequency is much higher than the line frequency, it can be assumed that the input voltage is constant during a switching period. In a boost converter the charge and discharge voltages of the inductor are:

$$\begin{aligned} v_{L(charge)} &= v_{in} \\ v_{L(discharge)} &= v_{in} - V_{out} \end{aligned} \tag{2}$$

where $v_{L(charge)}$ and $v_{L(discharge)}$ are the inductor voltages when the switching transistor is on and off respectively and v_{in} and V_{out} are respectively the input and output voltages.

Knowing that the charge current of the inductor is equal to the discharge current in steady state and, in order to obtain a stable inductor current, the following equation must be satisfied in continuous conduction mode (CCM):

$$\frac{v_{L(charge)} d_1 T_{sw}}{L} + \frac{v_{L(discharge)} (1 - d_1) T_{sw}}{L} = 0 \tag{3}$$

where L is the value of the inductor and T_{sw} is the switching period. Substituting (2) in (3) the first component of the duty cycle can be obtained as follows:

$$d_1(k) = \frac{V_{out} - v_{in}(k)}{V_{out}} \tag{4}$$

In the case of a dc-to-dc converter those values would be enough, but in our case of an ac-to-dc converter with PFC it is necessary to take into account the ripple of the output voltage:

$$v_{ripp} = \frac{P_{out}}{C \cdot \omega_r \cdot V_{out}} \sin(\omega_r t) \tag{5}$$

where C is the output capacity, ω_r is the pulsation of the voltage ripple, which is twice the line frequency, and P_{out} is the output power. Considering this output ripple, the first component of the duty cycle value is:

$$d_1(k) = \frac{(V_{out} - v_{ripp}(k)) - v_{in}(k)}{V_{out} - v_{ripp}(k)} \tag{6}$$

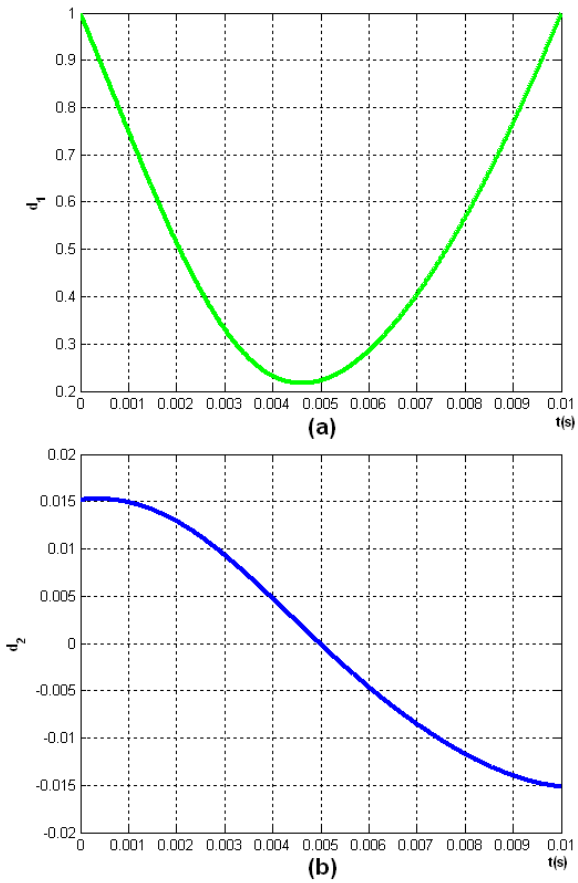

Fig. 3. Components d_1 and d_2 of the duty cycle during one half line period.

To achieve the best possible power factor it is necessary to consider a second component which is related with the energy stored in or released from the inductor (not considered in the first component), since the current is sinusoidal and rises up at the beginning of the half line period and decreases at the end. Let be the inductor voltage in a switching period *k* [6]:

$$V_L(t) = L\left(\frac{d_{iL}}{dt}\right) \approx \left(\frac{L}{T_s}\right)[i_L(k+1) - i_L(k)] \qquad (7)$$

then, the second component of the duty ratio is:

$$d_2(k) = \frac{\frac{L}{T_s}[i_L(k+1) - i_L(k)]}{V_{out} - v_{ripp}(k)} \qquad (8)$$

Those equations for *d(k)* are valid when the converter is in continuous conduction mode (CCM), as in the studied case. Because *d(k)* is the sum of the two components, the resultant duty cycle is slightly asymmetric. In the proposed method, the values of *d(k)* are calculated for a specific operation point. Those values are stored in a memory and used to generate the PWM signal, directly connected with the switching transistor of the converter.

TABLE I
PARAMETERS USED IN FIG.4. REAL AND IDEAL INPUT CURRENTS

V_{in} (V)	V_{out} (V)	L (mH)	C (µF)	P_{out} (W)	PF
55	100	5	200	37.5	0.9945

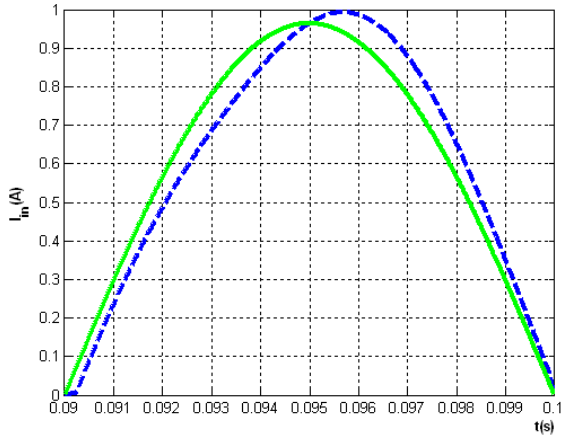

Fig. 4. Real and ideal input currents on the boost converter.

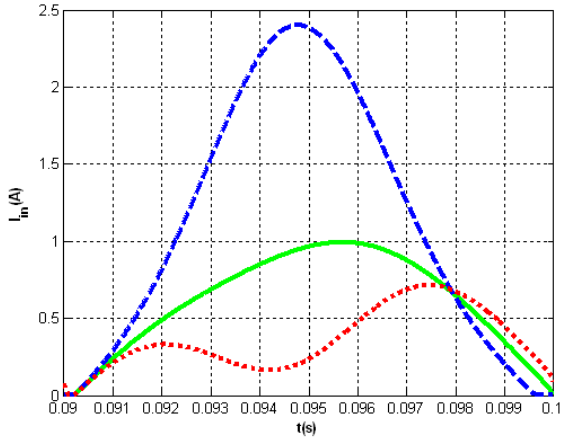

Fig. 5. Input currents for different output loads (see Table II).

TABLE II
PARAMETERS USED IN FIG.5. OUTPUT POWER VARIATION EFFECT

line	V_{in} (V)	V_{out} (V)	L (mH)	C (µF)	P_{out} (W)	PF
– –	55	100	5	200	75	0.9727
———	55	100	5	200	37.5	0.9945
·····	55	100	5	200	18.75	0.8338

It is important to take into account that ideal unity power factor can not be achieved. The first reason is that the calculated values of *d(k)* need to be stored in a memory, with the resulting quantization error. Secondly, the duty cycle should never be one to ensure a fixed switching period (T_{sw}), so it has been limited to a maximum of 0.95. This effect is shown in Fig. 4 where the continuous and dashed line represents the ideal and real current respectively in a boost converter with the parameters shown in Table I.

As mentioned before, the duty ratios are calculated for a specific operating point of input voltage and current, and output power. Fig. 5 shows the effect in the input current of varying the output power with respect to nominal conditions. In that figure, the continuous line represents the input current when the duty cycles are calculated for an output power of 37.5 W, the dotted and dashed lines are the input currents obtained when those duty ratios are applied to a load that consumes 18.75 W and 75 W respectively. The parameters used to obtain Fig. 5 are shown in Table II.

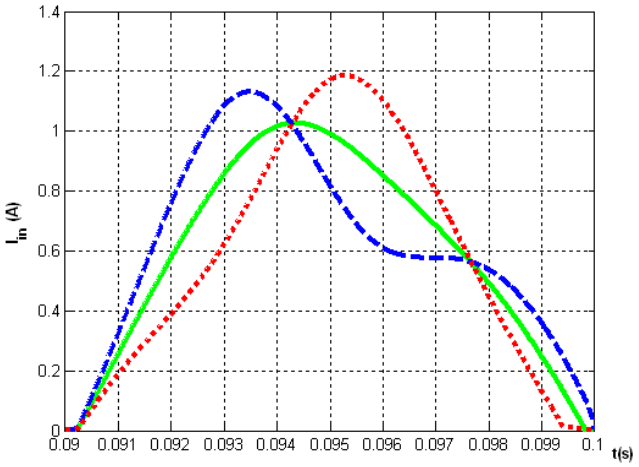

Fig. 6. Effect on the input current of the synchronization deviation (see Table III).

TABLE III
PARAMETERS USED IN FIG.6. SYNC DEVIATION EFFECT

line	V_{in} (V)	V_{out} (V)	L (mH)	C (µF)	α(º)	PF
———	55	100	5	200	0	0.9945
– – –	55	100	5	200	+0.2	0.9667
·····	55	100	5	200	-0.2	0.9804

The power factors obtained in Table II show that the control system works better when the power consumed by the load is higher than the nominal power. Therefore if it is desired to use the converter in a range of output powers with high power factors, the duty cycles should be calculated for the lowest power of the range.

In the technique presented in this paper the synchronization of the duty ratios with the line is a critical point. The deviation of the synchronization signal in even a few parts per thousand leads to a significant deterioration in power factor. The effect of this deviation is shown in Fig. 6, where the continuous line is the input current when the synchronization is ideally accurate, and the dotted and dashed line are the input current when the synchronization signal deviation (α) is + 0.2º and - 0.2º respectively. A negative deviation means that the sync signal is generated in the FPGA later than the zero cross of the input voltage, and vice versa. The parameters of each simulation and the resulting power factors are summarized in Table III.

It can be seen that positive synchronization deviation causes a greater deterioration of PF than a negative one at the same voltage and power conditions.

Another aspect that must be considered on the design is the power factor obtained in function of the inductance and capacitor values of the boost converter. Curves in Fig. 7 represent the input currents for different values of the inductor and sync deviations. Table IV summarizes the parameters used to obtain those figures.

From those simulations it can be concluded that the higher the value of the inductance, the better power factors achieved (at the same conditions), and the less sensitive to poor synchronization the system is. For that reason, the coil used in the simulations and experimental tests for this paper is oversized, so, if to achieve an input current ripple of 20% a 1.1 mH inductor is required, the boost is designed with a coil of 5 mH. To check the effects in the PF of the variation of the capacitor, similar tests to the previous one has been performed. Fig. 8 shows the input currents when different capacitors are used. The effect is similar to that produced when the coil value varies, but is less noticeable. As in previous cases, the test conditions are listed in the Table V.

In summary it can be concluded that to achieve a high power factor with this technique, the synchronization with the line must be as exactly as possible, the power operation conditions must be nominal or higher, and the inductance of the boost must be oversized.

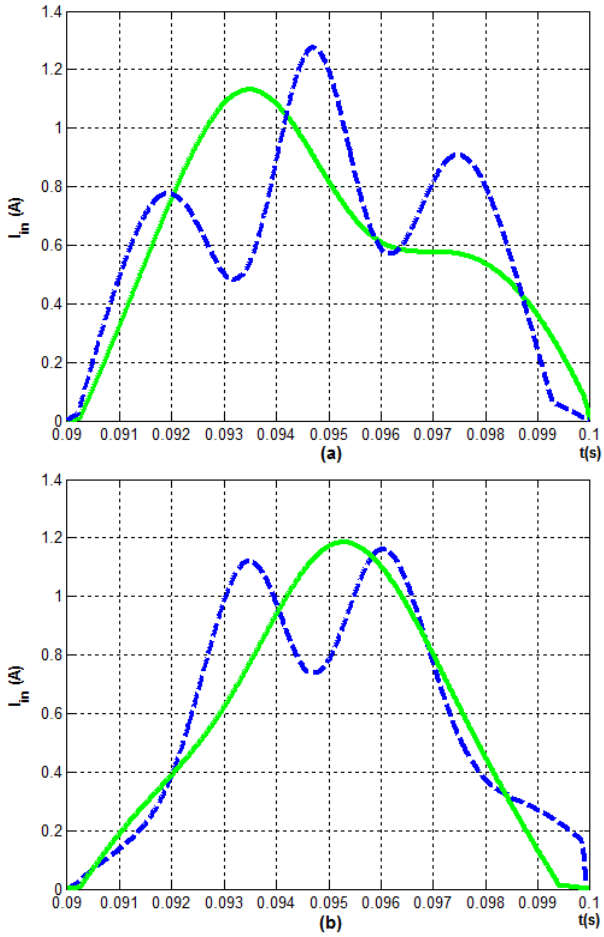

Fig. 7. Effect on the input current of different sync deviations and inductances (see Table IV).

TABLE IV
PARAMETERS USED IN FIG.7. COIL VARIATION EFFECT

Fig.	line	V_{in} (V)	V_{out} (V)	L (mH)	C (µF)	α(º)	PF
7.a	———	55	100	5	100	+ 0.2	0.9667
	– – –	55	100	1.1	100	+0.2	0.9609
7.b	———	55	100	5	100	- 0.2	0.9804
	– – –	55	100	1.1	100	- 0.2	0.9753

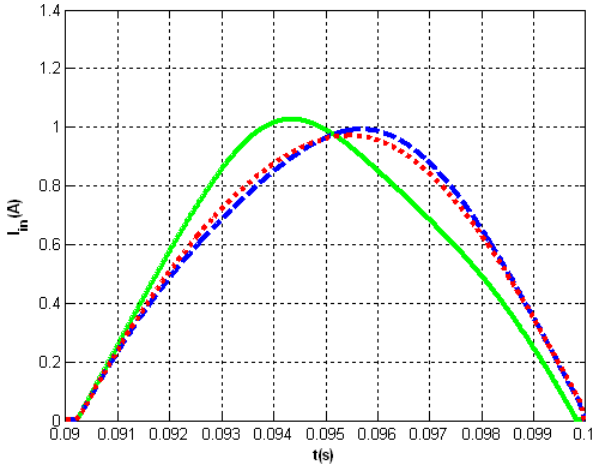

Fig. 8. Effect on the input current of different output capacitors (see Table V).

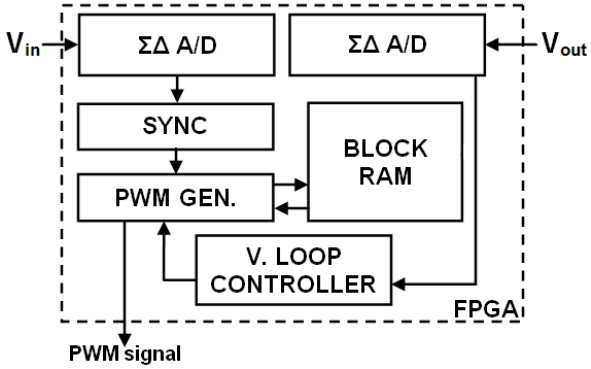

Fig. 9. VHDL implementation block diagram.

TABLE V
PARAMETERS USED IN FIG.8. CAPACITOR VARIATION EFFECT

line	V_{in} (V)	V_{out} (V)	L (mH)	C (µF)	α(°)	PF
———	55	100	5	100	0	0.9956
– – –	55	100	5	200	0	0.9945
·····	55	100	5	300	0	0.9971

III. VOLTAGE LOOP

As demonstrated in the previous chapter, neither current measurement nor current loop are needed in this method to achieve high PF, but to ensure stable output voltage an additional voltage loop is required. In a classic PFC scheme, as shown in Fig. 1, there are a voltage and a current loop. The first one has very slow dynamics and is responsible, varying the input conductance, for achieving an energetic balance between the input and output powers. The output voltage is compared to a reference voltage to obtain an error signal, which directly actuates on the current loop. The current loop has faster dynamics than the voltage one, and is responsible for making the input current proportional to the voltage, thereby correcting the power factor.

In the technique proposed in this paper, the voltage loop directly actuates on the duty cycle values, adding or subtracting a certain amount to obtain the desired output voltage. Since this loop changes the duty ratios, a slightly deterioration of the power factor is inevitable.

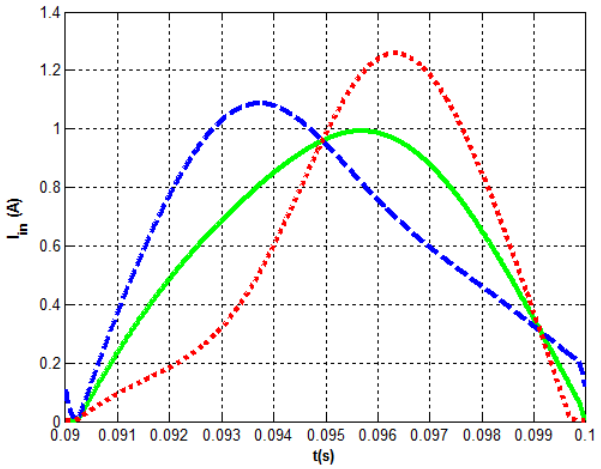

Fig. 10. Effect on the input current of different duty ratios (see Table VI).

TABLE VI
PARAMETERS USED IN FIG.10. DUTY RATIOS VARIATION EFFECT

line	V_{in} (V)	V_{out} (V)	L (mH)	C (µF)	d(k)	PF
———	55	100	5	200	+0 %	0.9945
– – –	55	100	5	200	+1 %	0.9789
·····	55	100	5	200	-1 %	0.9153

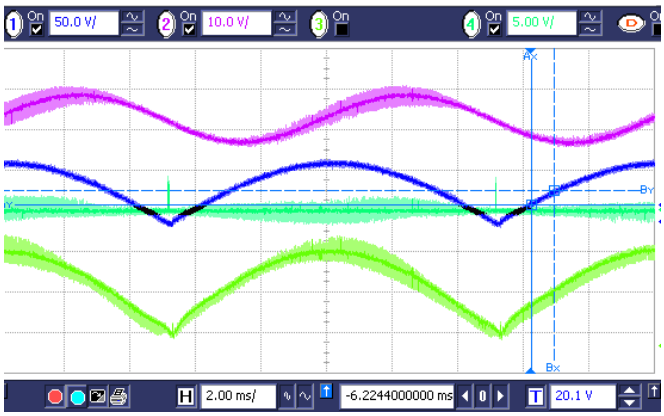

Fig. 11. Input and output voltages (blue and purple) (50 and 10 V/div. respectively) and input current (green) (1.06 A/div.) waveforms; $V_{in\text{-}rms}$ = 55 V, V_{out} = 100 V, P_{out} = 40 W. PF = 0.998. Voltage loop disabled.

In order to analyse the effects of the voltage loop in the resultant power factor, simulations have been performed. In those simulations a certain amount is added or subtracted to the original duty ratios. The parameters of those simulations are listed in Table VI, and the input currents are shown in Fig. 10. From the results it can be concluded that, when the duty cycles are modified, the resultant power factor is deteriorated, further when it is subtracted than when it is added.

IV. EXPERIMENTAL RESULTS AND DIGITAL IMPLEMENTATION

The method proposed in this paper was verified in an FPGA implementation. The FPGA's clock frequency is 100 MHz and the switching frequency is 100 kHz. The input voltage is measured in order to achieve the synchronization with the line, while the output voltage is measured for the

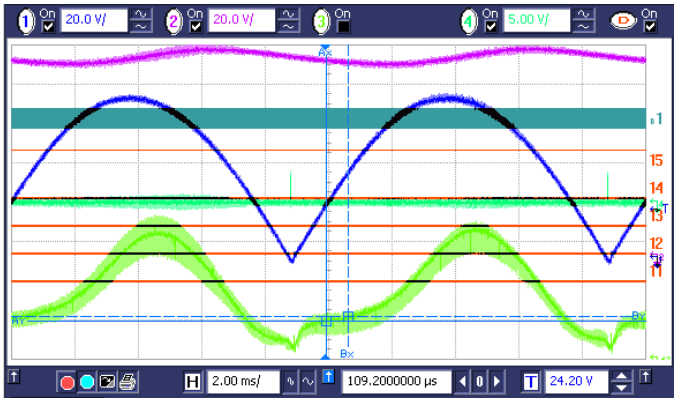

Fig. 12. Input and output voltages (blue and purple) (20V/div.) and input current (green) (0.53 A/div.) waveforms; $V_{in\text{-}rms}$ = 55 V, V_{out} = 100 V, P_{out} = 30 W. PF = 0.979. Voltage loop enabled.

voltage loop, but the input current is not measured. In the experimental tests, the input current has been measured trough a serial resistor of 4.7 Ω. Two ad-hoc sigma-delta 10-b A/D's have been implemented on the FPGA and can be easily integrated with the control system. The A/D's require few external components [8]; only a comparator and a first order R-C filter. The two measurements from the A/D's are connected to inputs on the FPGA, and the switching signal is connected to the switching transistor of the boost via a driver. The FPGA used is a Xilinx Spartan 3 XC3S200. The block diagram of the VHDL implementation of the proposed controller in FPGA is shown in Fig. 9. To implement the synchronization with the line a mechanism based on the rise and fall edges detection has been implemented and integrated in the FPGA. The complete controller, including the memory for the stored duty cycles, occupies 82.500 equivalent gates. Experimental results have been taken with the following conditions: V_{in} = 55 V, V_{out} = 100 V, P_{out} = 40 W, f_{line} = 50 Hz, f_{sw} = 100 kHz and f_{logic} = 100 MHz. The inductor value is 5 mH, and the output capacitor is 100 µF, the diode bridge is the FBL2504L, the MOSFET is the IRFP450 and the power diode is the DYV29-500. The experimental results are presented in the following sections.

A. Experimental results with voltage loop disabled

Tests in nominal and not nominal conditions have been performed. The input and output voltages and input current waveforms obtained when V_{in} = 55 V, V_{out} = 100 V and P_{out} = 40 W are shown in Fig.10. The power factor under this condition is 0.998.

B. Experimental results with voltage loop enabled

Tests in nominal and not nominal conditions have also been performed with the voltage loop enabled. The input and output voltages and input current waveforms obtained when V_{in} = 55 V, V_{out} = 100 V, P_{out} = 30 W are shown in Fig.12. The power factor under this condition is 0.979.

V. Conclusions

A digital controller for power factor correction has been proposed in this document. By calculating in advance the values of the duty ratios, neither current measurement nor current loop are required. Simulations to verify the effect in the input current of different parameters (such as inductor and capacitor values, synchronization deviation and output power ranges) have been performed. It has been found that, to achieve high power factor with the proposed technique, synchronization of the duty ratios with the line should be as accurate as possible, and the value of the inductor must be oversized, with respect to other control techniques. The duty ratios are calculated in a specific operating point of output power. If near unity power factors are required in a wider range, it is more appropriate to calculate the duty cycles in the lowest power. Both tests with voltage loop enabled and disabled have been performed. Because the voltage loop acts directly on the duty ratios, power factors are deteriorated when the voltage loop is enabled.

A prototype of a boost converter controlled by an FPGA based evaluation board, including the analog devices of the sigma-delta A/D's, was built to verify the proposed PFC method. Experimental results show the feasibility of the proposed method, obtaining high power factors in spite of not performing current measurements or current loop.

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