Paper submitted to IEEE Transactions on Power Electronics – Letters section - Manuscript ID TPEL-Letter-2009-06-0042

High Resolution FPGA DPWM based on Variable Clock Phase Shifting

Angel de Castro, *Member, IEEE*, Elías Todorovich

Universidad Autónoma de Madrid

Corresponding Author: Angel de Castro
Universidad Autonoma de Madrid
Escuela Politecnica Superior
Postal address:
Ciudad Universitaria de Cantoblanco
C/ Francisco Tomas y Valiente 11
28049 Madrid (SPAIN)
Tel. + 34 914972802
Fax. + 34 914974574
angel.decastro@uam.es

Part of this work was presented in the IEEE 39th Power Electronics Specialists Conference (PESC) 2008, Rhodes (Greece).

Keywords: digital control, field programmable gate arrays, pulse width modulation, signal resolution.

ABSTRACT

This paper proposes a very high resolution DPWM architecture that takes advantage of an FPGA advanced clock management capability: the fine phase shifting of the clock. This feature is available in almost every FPGA nowadays, allowing very small and programmable delays between the input and output clocks. An original use of this fine phase-shifting pushes the limits of DPWM resolution. The experimental results show a time resolution of 19.5 ps in a Virtex-5 FPGA.

I. INTRODUCTION

The insufficient resolution obtained in Digital Pulse Width Modulators (DPWM) has been one of the main obstacles to the expansion of digital control in the field of switching mode power supplies. DPWM resolution is a problem mainly for two reasons. The first one is that high DPWM resolution is needed in order to avoid limit cycling [1]-[2]. In fact, DPWM resolution needs to be higher than analog-to-digital converter (ADC) resolution to avoid this effect. Therefore, DPWM is an indirect limit to the precision of the measurement of the output voltage. The second reason is that DPWM resolution is inversely proportional to the switching frequency. This has made impractical the use of digital control for high switching frequencies (over 1 MHz).

Given this interest, many papers have appeared in the last few years studying alternatives on how to increase the resolution of DPWMs. A first group of studies focuses on the minimum time step that the DPWM can obtain, changing the hardware architecture of the DPWM [3]-[15]. A classification of these DPWMs has appeared [16], probably the most important criterion being the time quantization scheme: single-element time quantization (e.g. counter-based DPWM), 2^N-element time quantization (e.g. delay line based DPWM), and multiple-element time quantization (e.g. hybrid DPWM). The second group of studies tries to increase the effective duty cycle resolution changing the pattern used in the generation of the output signal. Digital dither [1], [13], sigma-delta [7], [12], [17], and slightly-changing frequency [18] are three good examples of this group. The present study is part of the first group, proposing a new architecture for reducing the minimum time step. To be precise, it is a hybrid DPWM. The proposed DPWM can be used with any of the techniques of the second group for increased resolution, as both groups are complementary. For example, the proposed DPWM can be enhanced using digital dither or sigma-delta techniques.

The rest of the paper is organized as follows: section II describes the proposed DPWM architecture. Section III shows the experimental results. Finally, section IV gives the conclusions.

II. PROPOSED DWPM ARCHITECTURE

A. Basic DPWM structure

The proposed DPWM takes advantage of the capability of field programmable gate arrays (FPGA) to shift the phase of the clock in small increments. Almost every FPGA nowadays includes this feature in its internal clock management system, which is used for synchronization with external memories among other applications. In the experimental results of this

paper, a Virtex-5 device from Xilinx® has been used. The resolution obtained is an order of magnitude beyond the resolution of other state-of-the-art proposals.

In Xilinx® FPGAs, the block that shifts the phase of the clock is called DCM (Digital Clock Manager). Apart from other features, such as frequency multiplication or division, the DCM includes the ability to shift the phase of the output clock with respect to the input clock using some additional control signals (see Fig. 1), basically a request-acknowledge protocol. This is called fine phase shift, an FPGA advanced feature on which the proposed DPWM is based. Its resolution is 1/256 of the input clock cycle or one tap delay of its internal delay locked loop (DLL), whichever is greater. The delay of a tap, according to the Virtex-5 datasheet, is between 7 and 30 ps. This resolution is, to the knowledge of the authors, finer than those of other state-of-the-art DPWMs [3]-[15]. Most of the previous results are in the order of 1 ns, with a few exceptions: 488 ps in [10], 390 ps in [12] and 255 ps in [11]. The resolution shown in the experimental results, 19.5 ps, goes well beyond these numbers.

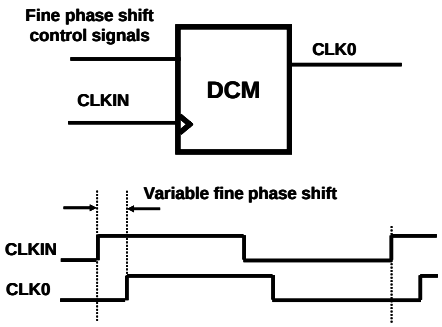


Fig. 1. DCM working: variable fine phase shift between CLKIN and CLK0.

Phase shifting in a DCM works as follows. The input clock is used as a time reference. Using the appropriate control signals, the relative phase of the input clock, *CLKIN*, and the output clock, *CLK0*, can be changed in steps of 1/256 of the clock period (see Fig. 1, variable fine phase shift). The DCM uses delay taps for adjusting the relative phase. In fact, the relative phase is adjusted to a number of delay taps that approaches the solution to the demanded phase as much as possible. Any resulting phase, obtained by single increment steps, from 0 to a full clock period is possible as long as the clock period is below the total delay of all the delay taps together.

The basic structure of the proposed architecture is shown in Fig. 2. It is a hybrid architecture in which the most significant bits (MSBs) of the duty cycle are handled in a synchronous block and the least significant bits (LSBs) in an asynchronous block.

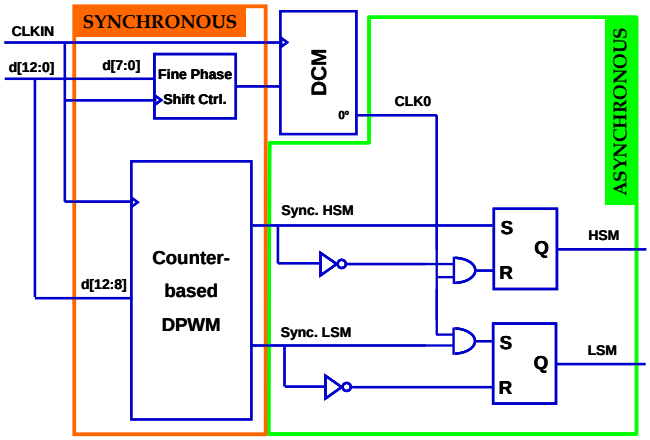


Fig. 2. Simplified architecture of the proposed DPWM.

The synchronous block, which manages the MSBs, is in fact a counter-based DPWM. If this block manages *M* bits, the internal counter ranges from *0* to 2^M*-1*. Whenever the *M* MSBs are below the value of the counter, the main output of this block (*Sync HSM*) is high, and low in the opposite case. This block is also in charge of the dead-times, and that is why a second output (*Sync LSM*) is included. If there were no dead-times, *Sync LSM* would simply be the inverse of *Sync HSM*. Dead-times are included to manage topologies with more than one switch, such as the synchronous buck converter. It is also important to note that the synchronous block uses the input clock, *CLKIN*, and not the shifted clock generated by the DCM. The reason will be apparent below.

The asynchronous block manages the LSBs. It uses 8 bits because the DCM of Xilinx® FPGAs has 256 steps of fine phase shift. The rest of the asynchronous block uses the clock *CLK0*, which is shifted with respect to *CLKIN* in all the possible range, from 0º to 360º, depending on the 8 LSBs. A simplified version of this block is shown in Fig. 2, which is valid for explaining how it works, but is not the complete circuit (see Fig. 5).

The way in which the DPWM output for the high side MOSFET (*HSM*) is generated is as follows (see Fig. 3). The MSBs determine the number of clock cycles that the output has to be active through *Sync HSM*, which is also the set signal of the RS latch at the output. The 8 LSBs are used for defining the fraction of clock cycle to be added at the output. These bits go to the block in charge of controlling the fine phase shift process, which is a finite state machine that shifts the *CLK0* clock by single steps until the phase between *CLKIN* and *CLK0* is equal to the fraction of clock cycle to be added. The RS latch is reset when the *CLK0* signal is active, but only after the set signal is already inactive (*and* gate, *inverter*). Therefore, the output signal (*HSM*) is active an integer number of clock cycles (determined by the MSBs) plus a fraction of clock cycle (determined by the LSBs).

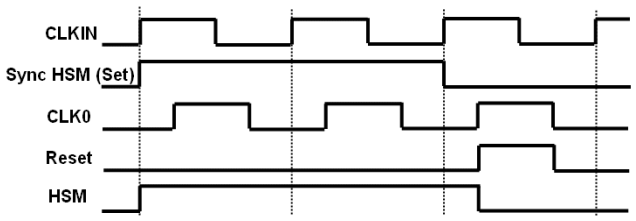


Fig. 3. HSM output generation.

A symmetric technique is used for generating the low side MOSFET output (*LSM*), using *CLK0* for the set of *LSM* and the synchronous signal *Sync LSM* (synchronized with *CLKIN*) for the reset.

B. Complete DPWM structure

This technique, as represented in Fig. 2, would not work for phases above 180º. In those cases, the reset signal would also be active at the beginning of the clock cycle, resetting the output before expected. This problem is shown in Fig. 4, which also shows the desired behavior in a discontinuous line. In order to avoid this problem, the real architecture is more complex than the one presented before. Fig. 5 shows the final architecture used in the asynchronous block. The synchronous block is not repeated for the sake of simplicity, but it has no changes. As can be seen, a register active at the rising edge of *CLK0* drives the reset signal of *HSM*, avoiding the problem.

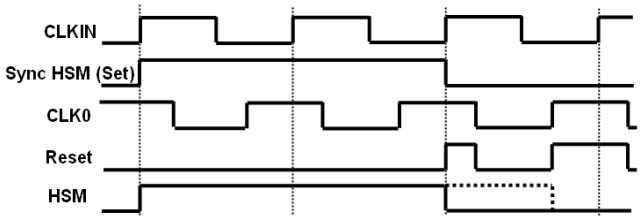


Fig. 4. HSM output generation problem for phases above 180º. Discontinuous line represents the desired behavior.

It could seem that the register that drives the reset signal of *HSM* is the only one necessary in Fig. 5, and that the multiplexer and the rest of registers are not necessary. This simplistic solution would be valid for ideal behavior, without taking into account delays. However, delays play a critical role in this circuit. The typical delay in a path inside an FPGA is in the order of 1 ns, which is much greater than the expected DPWM resolution (19.5 ps). Therefore, registers have been added for two reasons. One is to avoid the problem shown in Fig. 4 for phases near 0º or 180º, since the path delays can easily violate the setup time of two registers with similar phases. For instance, *CLKIN* and *CLK0* have similar phases when the phase is near but not equal to 0º. That is why different paths are used for phases under and above 180º. Each path includes a register driven by the opposite clock edge, so the setup time is not violated. The second reason is to enable

accurate delay equalization. Making a manual placement of the registers shown in Fig. 5, very accurate path equalization is obtained. The timing diagram of the proposed complete structure is shown in Fig. 6.

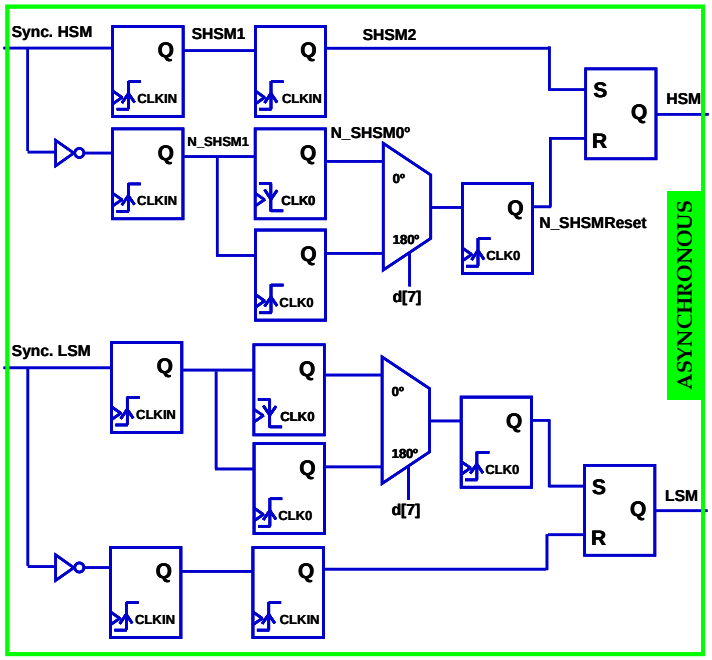


Fig. 5. Asynchronous block of the proposed DPWM.

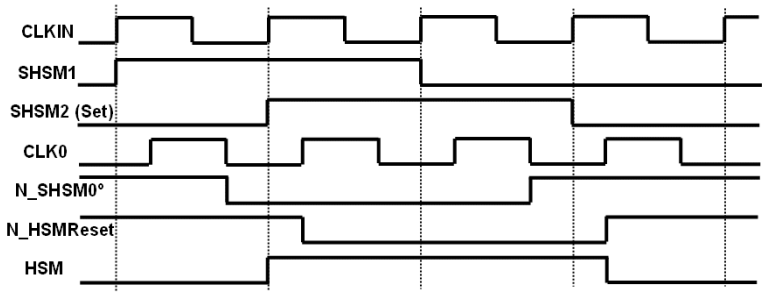


Fig. 6. HSM output generation using the complete structure.

C. Possible improvements

The main drawback of the proposed DPWM architecture is the phase shift update time. Each time that any of the 8 LSBs of the duty cycle changes, the phase of the output clock of the DCM must be changed. This is done through a request-acknowledge protocol in steps of 1/256 of the clock period. Using the prototype of the experimental results, it has been measured that this protocol can take up to 700 ns for a Virtex-5 FPGA. The 8 LSBs are managed changing the fine phase shift, so in the worst case 255 successive steps would be necessary (a change from 0º to almost 360º). If the update time is critical, a way of decreasing the phase shift update time is to use more than one clock. These clocks must have fixed phase

differences among them. In this way, the maximum phase shift is 360º/(number of clocks). Fig. 7 shows the basic structure when using 4 clock lines. The asynchronous block would be the one shown in Fig. 5, but using *CLK_SHIFTED* instead of *CLK0*. In that case, the maximum phase shift would be 90º and only 64 fine phase steps would be necessary. Taking into account that each DCM in Xilinx® FPGAs includes 4 clock outputs phase-shifted by 0º, 90º, 180º and 270º, and that most FPGAs have between 2 to 8 DCMs, the maximum phase shift can be drastically reduced if necessary.

The phase shift update time affects only the transient behavior. During a transient, the maximum error can be up to the clock period divided by the number of clocks used. In any case, the MSBs are changed immediately, so the transient error is relatively small.

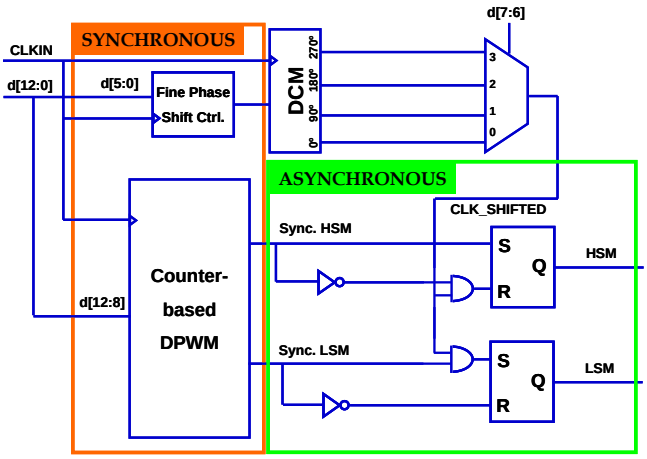


Fig. 7. Proposed architecture when using more than one clock.

III. EXPERIMENTAL RESULTS

The proposed architecture has been designed in VHDL and implemented in a Virtex-5 (XC5VFX30T-1FFG665) Xilinx® FPGA. The Virtex families are formed by high-end FPGAs. Virtex-5 has been chosen to show the best currently achievable performance. The target application has been a 4-phases synchronous buck converter. Therefore, each DPWM has been replicated four times, one for each phase. Almost identical results have been obtained in the four phases, showing that the proposed DPWM can be accurately replicated. For the sake of simplicity, all the results are shown for a single phase, in order to avoid repeating the same graphs four times.

An external clock at 100 MHz is internally multiplied to 200 MHz. The switching frequency is 6.25 MHz, obtaining 13 bits of resolution (5 in the synchronous block and 8 in the asynchronous one). Fig. 8 shows the experimental waveforms with a duty cycle of 0.5 for the HSM (upper part). The signal for the LSM (lower part) has a duty cycle under 0.5 because of

the dead-time. The time step resolution is 1/256 of the internal 200 MHz clock period, that is, 19.5 ps. In order to obtain the same resolution with a counter-based DPWM, a 51.2 GHz clock would be necessary. It must be taken into account that the obtained resolution is very similar to usual values of clock jitter. For instance, the oscillator used in the experiments, F4105-1000, has a cycle-to-cycle jitter of 20 ps, while the DCM of Virtex-5 guarantees a maximum clock synthesis period jitter of 120 ps. Therefore, the obtained resolution of 19.5 ps must be understood as a mean value, that is, the mean duty cycle changes about 19.5 ps every single step. However, cycle-to-cycle changes that significantly differ from 19.5 ps must be expected due to clock period inaccuracies.

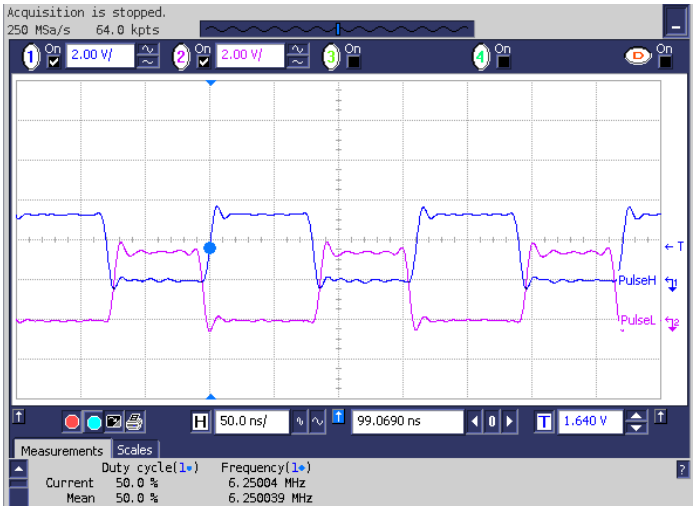
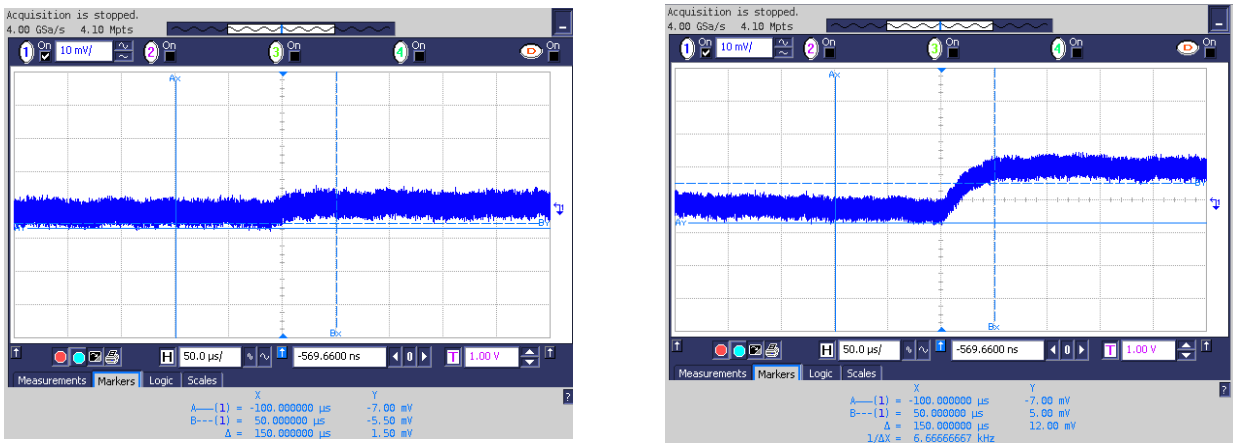


Fig. 8. Experimental waveforms at 6.25 MHz. Upper signal, pulse for the HSM, lower signal, pulse for the LSM.

In order to show the achieved resolution, the PWM signal has been connected to an UCC37324 driver powered at 12 V whose output feeds an RC filter (1 kΩ, 22 nF). Fig. 9a shows a 1 bit step in the duty cycle command. The expected change in the output voltage would be $12/2^{13}$ V, i.e. 1,47 mV, similar to the experimental result (about 1.5 or 2 mV), a very high resolution in spite of having a switching frequency of 6.25 MHz. It can be appreciated that the mean value changes as expected, but there are also other minor fluctuations that can be attributed to multiple jitter sources. Fig. 9b shows a step of 8 units in the duty cycle command, so the expected step would be 8 times larger, i.e. 11.72 mV, very similar to the experimental result of about 12 mV.



a b

Fig. 9. Step response connecting the PWM signal to a driver feeding an RC filter. 50 µs/div, 10 mV/div. a) 1 unit step, b) 8 units step.

Fig. 10 shows the results of the proposed DPWM in all the duty cycle range. The horizontal axis represents the duty cycle expressed as an integer number instead of a fraction: 13 bits of resolution, so the duty cycle goes from *0* to $2^{13}-1$ (8191). The vertical axis represents the on time of *HSM* in ps. The upper part of Fig. 10 shows the complete duty cycle range. Very high linearity is appreciated, as expected, because the 5 MSBs are used in a counter, which is a highly linear component. It is more interesting to see the detailed behavior when changing the 8 LSBs, so the small 19.5 ps steps can be appreciated. The lower part of Fig. 10 shows the on time when the duty cycle changes from 1279 (4FF in hexa) to 1536 (600 in hexa), which is a complete clock cycle (500 to 5FF in hexa) plus their adjacent values. High linearity is also observed, but the resolution is so high (19.5 ps) that it is difficult to make precise measurements. A 4 GSps oscilloscope (Agilent 54831D) has been used, taking the mean value after at least one thousand measurements at each point.

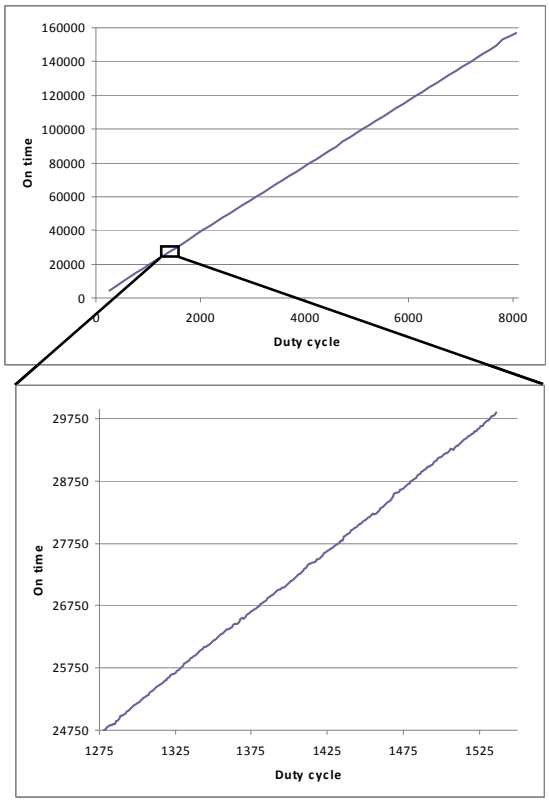


Fig. 10. On time versus duty cycle. Upper part, complete duty cycle range. Lower part, zoom detail along a clock cycle.

IV. CONCLUSIONS

A hybrid DPWM based on fine clock phase shifting has been proposed. The architecture uses FPGA advanced clock management capabilities to obtain a very high resolution. The time step is so small that manual placement is necessary in the asynchronous part of the design. The DPWM has been described in VHDL and implemented in a Virtex-5 FPGA. The experimental results show the feasibility of the method, obtaining good linearity with a time step of 19.5 ps.

V. REFERENCES

[1] A.V. Peterchev, S.R. Sanders, "Quantization resolution and limit cycling in digitally controlled PWM converters," *IEEE Trans. Power Electron.*, vol. 18, n. 1, pp. 301-308, Jan. 2003.

[2] H. Peng, A. Prodic, E. Alarcon, D. Maksimovic, "Modeling of quantization effects in digitally controlled DC-DC converters," *IEEE Trans. Power Electron.*, vol. 22, n. 1, pp. 208-215, Jan. 2007.

[3] A.P. Dancy, A.P. Chandrakasan, "Ultra low power control circuits for PWM converters," in *Proc. IEEE Power Electronics Specialists Conf. (PESC)*, June 1997, St. Louis, Missouri, USA, vol. 1, pp. 21-27.

[4] A.V. Peterchev, J. Xiao, S.R. Sanders, "Architecture and IC implementation of a digital VRM controller," *IEEE Trans. Power Electron.*, vol. 18, n. 1, pp. 356-364, Jan. 2003.

[5] E. O'Malley, K. Rinne, "A programmable digital pulse width modulator providing versatile pulse patterns and supporting switching frequencies beyond 15 MHz," in *Proc. IEEE Applied Power Electronics Conf. Expo (APEC)*, vol. 1, Feb. 2004, Anaheim, CA, pp. 53-59.

[6] R.F. Foley, R.C. Kavanagh, W.P. Marnane, M.G. Egan, "An area-efficient digital pulsewidth modulation architecture suitable for FPGA implementation," in *Proc. IEEE Applied Power Electronics Conf. Expo (APEC)*, Mar. 2005, Austin, TX, vol. 3, pp. 1412-1418.

[7] Z. Lukic, N. Rahman, A. Prodic, "Multibit Σ–Δ PWM digital controller IC for dc–dc converters operating at switching frequencies beyond 10 MHz," *IEEE Trans. Power Electron.*, vol. 22, n. 5, pp. 1693-1707, Sep. 2007.

[8] K. Wang, N. Rahman, Z. Lukic, A. Prodic, "All-digital DPWM/DPFM controller for low-power DC-DC converters," in *Proc. IEEE Applied Power Electronics Conf. Expo (APEC)*, Mar. 2006, Dallas, TX, pp. 719-723.

[9] V. Yousefzadeh, T. Takayama, D. Maksimovic, "Hybrid DPWM with digital delay-locked loop," in *Proc. IEEE Computers in Power Electronics Workshop (COMPEL)*, July 2006.

[10] T. Carosa, R. Zane, D. Maksimovic, "Scalable Digital Multiphase Modulator," *IEEE Trans. Power Electron.*, vol. 23, n. 4, pp. 2201-2205, Jul. 2008.

[11] R. Foley, R. Kavanagh, W. Marnane, M. Egan, "Multiphase digital pulsewidth modulator," *IEEE Trans. Power Electron.*, vol. 21, n. 3, pp. 842-846, May 2006.

[12] Z. Lukic, C. Blake, S.C. Huerta, A. Prodic, "Universal and fault-tolerant multiphase digital PWM controller IC for high-frequency DC-DC converters," in *Proc. IEEE Applied Power Electronics Conf. Expo (APEC)*, Feb. 2007, Anaheim, CA, pp. 42-47.

[13] J. Zhang, S.R. Sanders, "A digital multi-mode multi-phase IC controller for voltage regulator application," in *Proc. IEEE Applied Power Electronics Conf. Expo (APEC)*, Feb. 2007, Anaheim, CA, pp. 719-726.

[14] S.C. Huerta, A. de Castro, O. Garcia, J.A. Cobos, "FPGA based digital pulse width modulator with time resolution under 2 ns," *IEEE Trans. Power Electron.*, vol. 23, n. 6, pp. 3135-3141, Nov. 2008.

[15] M.G. Batarseh, W. Al-Hoor, L. Huang, C. Iannello, I. Batarseh, "Segmented digital clock manager – FPGA based digital pulse width modulator technique," in *Proc. IEEE Power Electronics Specialists Conf. (PESC)*, Jun. 2008, Rhodes, Greece, pp. 3036-3042.

[16] A. Syed, E. Ahmed, D. Maksimovic, E. Alarcon, "Digital pulse width modulator architectures," in *Proc. IEEE Power Electronics Specialists Conf. (PESC)*, vol. 6, Jun. 2004, Aachen, Germany, pp. 4689-4695.

[17] A. Kelly, K. Rinne, "High resolution DPWM in a DC-DC converter application using digital Sigma-Delta techniques," in *Proc. IEEE Power Electronics Specialists Conf. (PESC)*, vol. 6, Jun. 2005, Recife, Brazil, pp. 1458-1463.

[18] J. Li, Y. Qiu, Y. Sun, B. Huang, M. Xu, D.S. Ha, F.C. Lee, "High resolution digital duty cycle modulation schemes for voltage regulators," in *Proc. IEEE Applied Power Electronics Conf. Expo (APEC)*, Feb. 2007, Anaheim, CA, pp. 871-876.