Handling input voltage frequency variations in power factor correctors with precalculated duty cycles

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***Abstract*—The use of precalculated duty cycles for power factor correction leads to a significant simplification of the design and a reduction of the final cost. There are previous proposals for handling non-nominal conditions such as input voltage or load variations. However, there are no proposals for handling input frequency variations, which have an important impact in the power factor. This paper measures this impact and includes a simple loop to handle the variations of the input frequency. The results show that the introduction of this loop keeps the power factor values around those obtained in nominal conditions.**

Keywords—PFC; FPGA; Frequency robustness

I. INTRODUCTION

The initial approach to power factor correction (PFC) implies sensing both the input and output voltages and the input current. Analog proposals have provided cheap and functional solutions for several years. However, the lowering of prices of digital devices and their ease of use have increased their application to PFC. Digital solutions rely on different type of devices for this task. Literature shows examples of the utilization of microcontrollers [1], digital signal processors [2] and FPGAs [3] for solving PFC.

Although digital devices have demonstrated enough capability for dynamically calculating the actuation in real time [4], these solutions require different analog to digital converters, increasing the cost of the digital solution. To reduce costs and to simplify the design of the controller, several works avoid input current measurement by using input and output voltage information [5, 6, 7]. Literature also presents examples of current measurement avoidance by means of precalculating the duty cycles and detecting the zero-crossing of the input voltage to synchronize the controller:

Several authors have proposed different solutions using the precalculated approach. In [8, 9], a set of eight different precalculated vectors is used to handle output voltage variations. The solution proposed in [10] generates the duty cycle values for a half-line period in the previous one, considering the input and output voltages measured during the last period. Finally, in [11] the duty cycle values are divided into three different factors. These factors are modified considering the output voltage measurement to handle some variations from nominal values.

Previous works focused on handling variations in the output voltage due to load or input voltage changes while preserving the power factor. This work focuses on the performance of a precalculated system when the frequency of the input voltage differs from the nominal value. The standard EN50160 [12] describes the low-voltage supply characteristics. The power frequency for interconnected supply systems is 50 Hz ± 1 % during 99.5 % of a year and a frequency of 50 + 4 % / - 6 % during 100 % of the time. Although frequency changes are small, they have an important impact in the obtained power factor using precalculated techniques.

This paper is divided as follows. Section II describes the modifications made to a precalculated duty cycle regulator to handle frequency variations. Section III shows the experiments performed with the new implementation. Section IV presents a discussion about the obtained results. Finally, section V summarizes this work.

II. DEVELOPMENT

This work improves the functionality of the precalculated duty cycle regulator presented in [11]. This regulator has been created for controlling a boost converter. This regulator has been designed to be implemented using a 100 MHz FPGA. The relation between the clock period (10 ns) and the utility period (10 ms) is 10^6. The same relation must be fulfilled between the number of PWM cycles and the number of clock pulses per PWM cycle. The chosen PWM resolution is 1000 clock pulses. Hence, the nominal utility period is divided into 1000 PWM cycles. For each of these cycles, the PWM duty cycle has been calculated and stored in a look-up-table (LUT). The restart of the precalculated sequence of duty cycles has to be synchronized to the start of a new utility period. This is achieved thanks to a comparator module. This module measures the time that the rectified input voltage (V_g) is below a defined threshold. Considering the symmetry of V_g the zero-crossing instant occurs at the half of the measured period. Using this information, the regulator generates a synchronization signal which restarts the indexation of the LUT. Fig. 1 shows a simplified diagram of the existing PFC controller.

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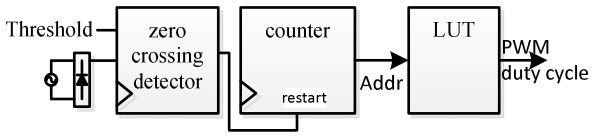


Fig. 1. Diagram of the existing controller for PFC.

The proposal of this paper is to include a frequency loop to modify the number of precalculated duty cycles applied in each utility period. This frequency loop measures the time between consecutive restart signals to measure the duration of the utility period. These measurements are recorded into a 32 position shift register. The regulator can be configured to consider the last measurement or the average of a set of them (2, 4, 8, 16, 32). Also the regulator can be configured to use all of them or segregate the positive utility periods from the negative utility periods. These two options, the number of utility periods considered and the segregation of positive from negative, can be freely combined. This information defines the number of PWM cycles that must be applied to the utility period. The difference between this measurement and the nominal value (1000) is the number of PWM cycles that must be removed (for higher frequencies) or inserted (for lower frequencies). The absolute value of this difference is in the range [0, 60], corresponding to the variation of a 6% of the frequency. The module equally distributes the positions where the PWM cycles are to be removed or inserted. For this task, the new module uses a LUT which stores, for each value of this difference the index of the first PWM cycle to be modified. The list of PWM cycles indexes to be modified is obtained adding the stored value to the last modified index. The position of these indexes within the original vector is depicted in Fig. 2.

When the frequency of the input voltage is higher than the nominal value, the module must remove PWM cycles. Therefore, the frequency regulation module will skip the PWM duty cycle corresponding to the ones included in the list presented before. Otherwise, when the frequency of the input voltage is lower than the nominal value, the module must insert new PWM duty cycles. These new duty cycles are repetitions of those cycles that are in the list of the indexes to be modified. As it is depicted in Fig. 3, the modifications to the existing PFC controller are minimal. The former counter is replaced by the frequency regulation module which uses the same information as the counter and provides the address of the PWM duty cycle to be retrieved from the same LUT.

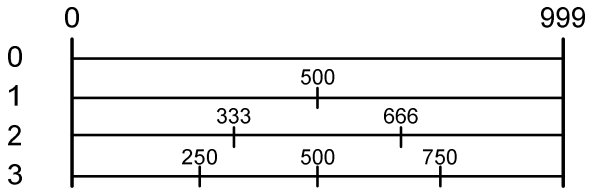


Fig. 2. Diagram of the controller for PFC including the new module for frequency regulation..

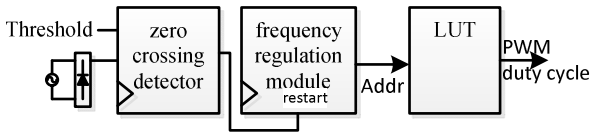


Fig. 3. Diagram of the controller for PFC including the new module for frequency regulation.

The proposed solution requires less resources than storing different duty cycle vector for the different frequencies that the input voltage may present. This modification is also simpler than dynamically generating a new duty cycle vector for the new frequency. This modification would require the access to the original LUT information to interpolate the value of the new duty cycle to be inserted or to modify several duty cycle values to smooth the removal of one.

III. Experiments

The experiments have been carried out over a boost converter (L = 5 mH, C = 68 μF, P = 300 W, V_g = 230 V, V_{out} = 400 V, fsw = 100 kHz). The controller has been implemented using an FPGA Xilinx XC3S1000-4FT256. The clock frequency of the system is 100 MHz. The utility period has been divided into 1000 PWM cycles. For each of these cycles, the PWM may be set to a duty cycle from 0 to 999. The values of the 1000 switching cycles have been precalculated offline and stored in the FPGA.

The power source used in the experiments is a Pacific Power Source 115-ASX. This power source not only allows modification of the AC frequency provided to the converter but it also provides a real time measurement of the power factor.

The experiment has measured the power factor of the boost converter when the AC frequency has been set to the nominal value (50 Hz) and also modified to a ± 2% and a ± 4%. For each of these five different frequencies, Table I shows the PF obtained using:

a) The original precalculated regulator, which applies a precalculated duty cycle controller without any frequency correction.

b) The frequency loop modifying the duty cycle vector considering the frequency measured in the last utility period.

c) The frequency loop modifying the duty cycle vector considering the frequency measured in the last equivalent utility period (segregating the positive utilities from the negative ones).

d) The frequency loop modifying the duty cycle vector considering the average between the last two utility periods (one positive and one negative).

A second experiment evaluated the use of the average value of a larger set of measurements. The measured frequency value in steady state has a variability of 0.1 %. This variation implies the addition or subtraction of only one duty cycle. This little variation is not significant to modify the resulting average.

TABLE I. THIS TABLE PRESENTS THE POWER FACTOR VALUES FOR THE DIFFERENT INPUT VOLTAGE FREQUENCIES (NOMINAL, ± 2% AND ± 4%) AND THE FOUR PROPOSED CONTROLLING METHODS

	Input Voltage Frequency				
	48 Hz	***49 Hz***	***50 Hz***	***51 Hz***	***52 Hz***
Former precalculated PFC controller	0.78	0.915	0.982	0.942	0.856
Freq. loop using last measure	0.96	0.97	0.955	0.969	0.96
Freq. loop using last equivalent measure	0.992	0.992	0.995	0.992	0.992
Freq. loop using the average of the last two measures	0.98	0.98	0.98	0.98	0.977

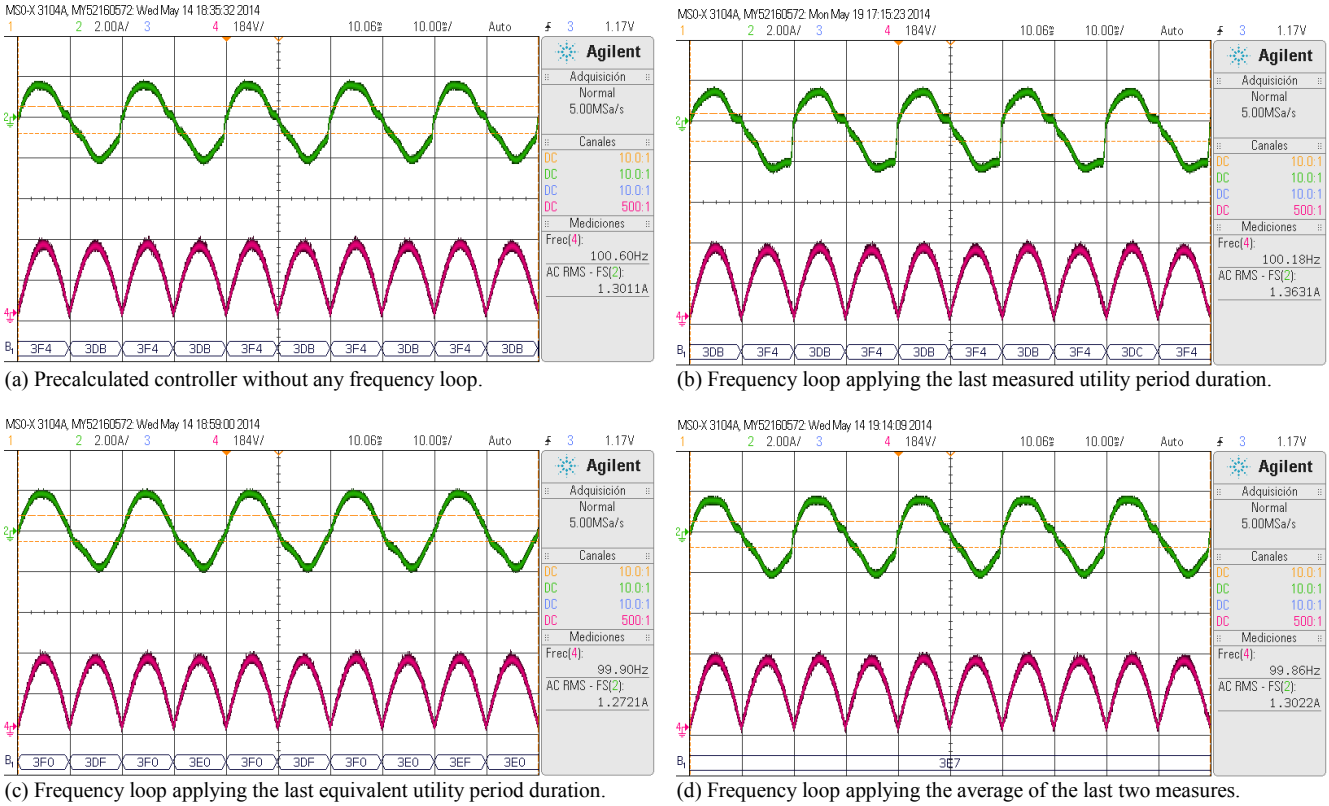
Therefore, the results of this experiment have not been included in the paper.

IV. DISCUSSION

The first point of discussion is the performance of the four methods in nominal conditions. Fig. 4 shows the current measures and the duration of each utility period. Theoretically, the original controller should provide the best PF values in nominal conditions. However, as it was presented in Table I, the original controller provides a PF of 0.982 and the option c) which includes the frequency loop using the last equivalent measure provides a PF of 0.995.

It can be observed in Fig. 3a that the duration of consecutive utility periods is not the same, being 1012 PWM cycles for the positive utility periods and 987 PWM cycles for the negative utility periods. This controller was designed for utility periods lasting 1000 PWM cycles. Therefore, a ± 1% error is being introduced. When the frequency loop uses the last measured information is applying 987 PWM cycles for a utility period that lasts 1012 PWM cycles, the error is duplicated. For this reason, the results of this option (Fig. 3b) are even worse than the ones obtained using the original regulator. The best result is obtained when the frequency loop uses the values obtained measuring the previous equivalent utility period. In this case, the controller adapts the original 1000 PWM cycles vector to the new frequency, repeating some of them to achieve 1012 cycles or removing some to achieve 987 cycles. Finally, when the frequency loop uses the average value of the last two utility periods (Fig. 4c shows a value of 999), the frequency loop only removes one PWM cycle from the original vector. This modification shows no significant modification to the PF compared to the result obtained with the former controller, as it is using the same number of PWM cycles for the utility period.

This lack of symmetry is usually observed when using AC power sources. The difference is less significant in the electrical grid. However, it still occurs so a distinguishing positive and negative utility periods is recommended.



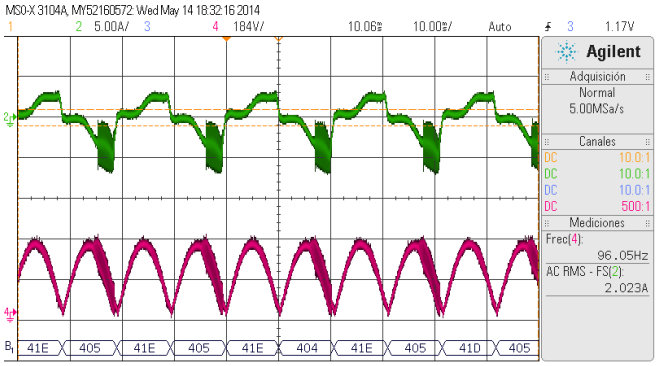
(a) Precalculated controller without any frequency loop.

(b) Frequency loop applying the last measured utility period duration.

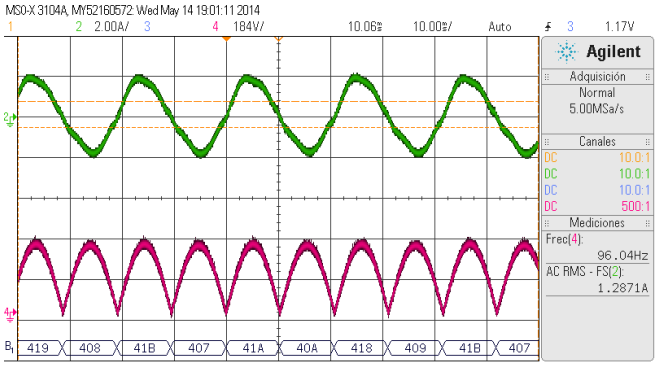
(c) Frequency loop applying the last equivalent utility period duration.

(d) Frequency loop applying the average of the last two measures.

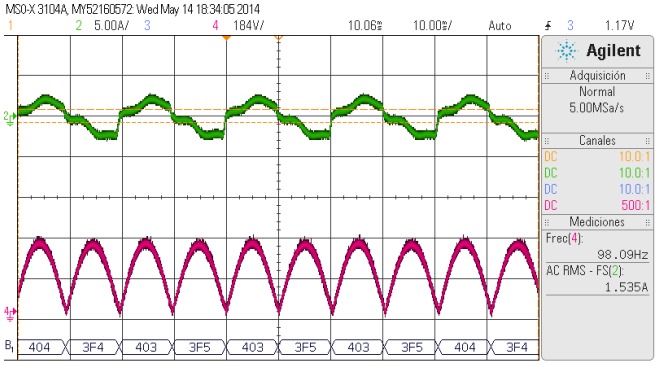
Fig. 4. Comparison of the four methods in nominal conditions. The upper analog signal is the input current, the lower analog signal is the rectified input voltage. The digital signal is the hexadecimal value corresponding to the number of PWM cycles that the frequency loop will use for the corresponding utility period (1000_d corresponds to $3E8_h$).



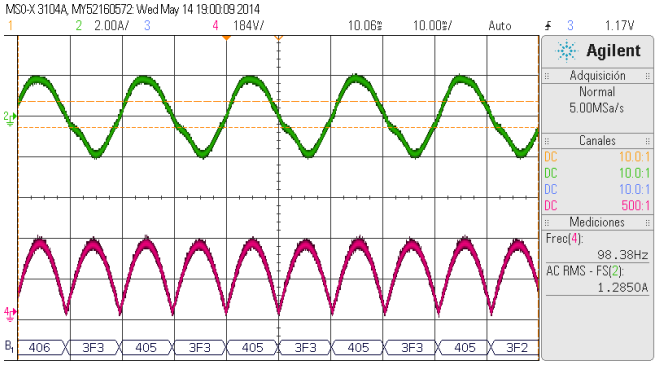
(a) Precalculated controller at 48Hz.



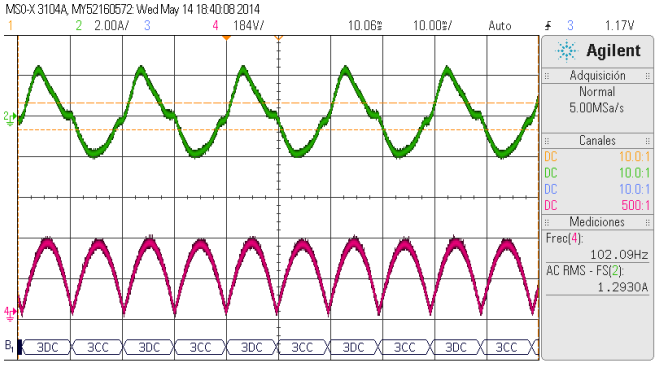
(b) Frequency loop at 48 Hz.



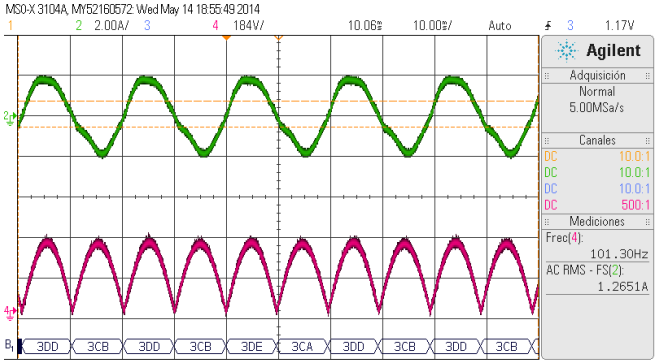
(c) Precalculated controller at 49Hz.



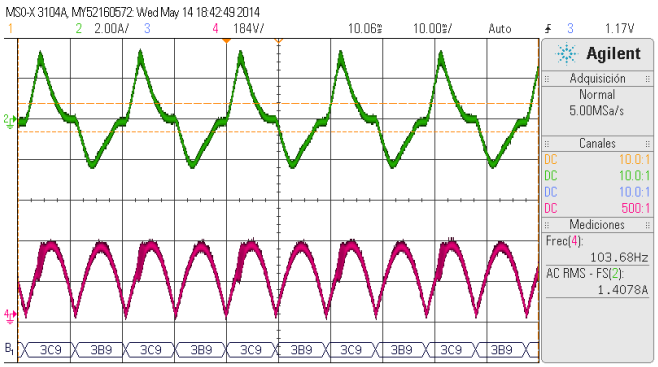
(d) Frequency loop at 49 Hz.



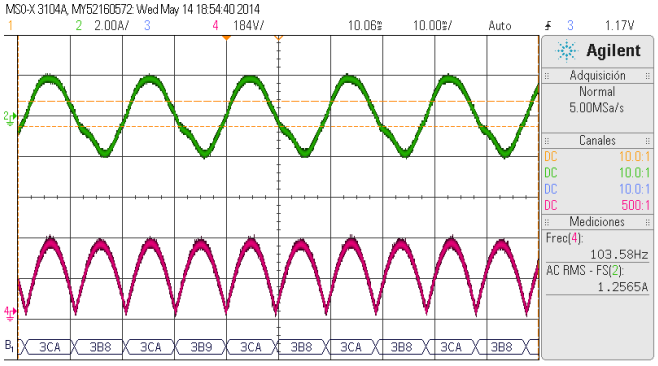
(e) Precalculated controller at 51Hz.



(f) Frequency loop at 51 Hz.



(g) Precalculated controller at 52Hz.



(h) Frequency loop at 52 Hz.

Fig. 5. Comparison of the former precalculated controller (subfigures a, c, e and g) and using the frequency loop (subfigures b, d, f, h). These two controllers are compared for the following input voltage frequencies: 48 Hz, 49 Hz, 51 Hz, 52 Hz. The upper analog signal is the input current, the lower analog signal is the rectified input voltage. The digital value is the number of PWM cycles that the frequency loop will use for the corresponding utility period.

The second point of discussion is the performance of the original controller versus the application of the proposed frequency loop in non-nominal conditions. For this comparison, Fig. 5 presents the measurements of the original controller and the best results of the frequency loop, i.e. using the measure of the last equivalent utility period. This figure includes the behavior of the input current for the ± 2% and for the ± 4% input voltage frequency variations. As it was expected, the deterioration of PF when using the original controller is significant. However, this deterioration is not symmetrical, as the behavior is significantly worse when the input voltage presents lower frequencies (PF is lower than 0.8 when input voltage frequency is 48 Hz). On the other hand, the obtained PF when the frequency loop is working is almost the same for both nominal and non-nominal conditions. This PF is slightly higher when the systems is working on nominal conditions, but the difference is not significant.

The results presented in Fig. 5 also show the lack of symmetry between the positive and negative utility periods. However, either using the last measurement or the average of the last two measurements (i.e. options presented as b) and c) in the previous section) provides better results than the original controller. The modification that the loop introduces in the application of the PWM duty cycle vector provides some correction for the variation of the input voltage frequency.

V. Conclusion

This work proposes the use of a simple frequency loop for precalculated PFC controllers. These controllers rely on a precalculated vector of PWM duty cycles that are applied along the utility period. The frequency loop modifies the sequence of these PWM duty cycles inserting or removing elements to fit to the measured duration of the utility period. The proposed modification requires minimal modification to the existing controller as it only modifies the address of the LUT which contains the PWM duty cycle vector.

The experiments show that this frequency loop keeps the PF of the switching converter when the input voltage frequency is not in nominal conditions. The use of the frequency loop is also recommended even for nominal conditions as it has proven to increase the PF. It can be observed that some lack of precision in controllers clock signal, the lack of symmetry of the power source or in the diode bridge result on a deterioration of the PF. Including the frequency loop has increased the PF and kept it constant in non-nominal AC frequencies.

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