High Efficiency Si Solar Cells Characterization Using Impedance Spectroscopy Analysis

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High Efficiency Si Solar Cells Characterization Using Impedance Spectroscopy Analysis

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Abstract. Impedance Spectroscopy has been used to analyse commercial Si photovoltaic solar cells, to obtain information about minority carrier lifetimes, series and parallel resistances, and acceptor impurity densities. Silicon solar cells efficiencies ranging between 17 and 18% from different manufacturers have been analysed obtaining differences mainly in the electron lifetimes and doping densities. Relations between these parameters and DC curves are discussed.

1. Introduction

Silicon solar cells and panels still remain as the most used for the installation of photovoltaic power plants due to their reduced cost and mature fabrication process. New cells are produced with increasing efficiencies by means of the introduction of ameliorated processing techniques as well as improvements in material quality. Determining the characteristics of the performance of those solar cells is essential to improve their optimization.

Among other techniques, Impedance spectroscopy, as an AC characterization technique has been recognized as a valuable tool to obtain the transient response of charge carriers [1], which is not available when using only DC characterization. Bias dependent capacitance is one of the proposed techniques to obtain information on interface defects and on the carrier lifetime due to the fact that biasing or illuminating changes device dynamics, and that change becomes visible through capacitance variation.

The aim of this work is using impedance spectroscopy (IS) in commercial photovoltaic (PV) solar cells to compare their performances.

2. Experimental

PV cells used in this study were four commercial polycrystalline Si solar cells from different manufacturers, and with nominal efficiencies in the range of 17-18%, except sample C with 14%.

IV curves were obtained using a Cell tester from NPC Incorporated, model NPC 180 15 BPS. The system produces illumination from 0.5 to 1 sun (AM1.5G) and keeps a constant temperature of 25ºC by means of a peltier cooler, avoiding heating effects due to illumination. Solar cell biasing was applied between -0.1V to 0.7V, to go from I_{sc} (0V) to slightly higher voltage values than V_{oc}.

Impedance measurements were performed using a HP4284 LCR meter from 20Hz to 1MHz with a small AC signal of 20mV (rms). Bias voltages ranged from -2V to 1V producing impedance curves. Measurement setup has been characterized to be able to simulate our AC networks taking into account the parasitic resistances and inductances at high frequencies. The obtained parameters were a resistance of 9Ω and an inductance of 5μH. Even they produced almost negligible effects when fitting the data to the equivalent circuits, those were taken into account in every sample.

Silicon solar cells capacitance shows two main components as a function of bias [2]: a Mott–Schottky characteristic, due to the modulation of the Schottky barrier, at reverse and moderate forward bias, and a chemical capacitance [3], that increases exponentially for intense forward bias.

Two main processes are responsible of carrier extraction in crystalline solar cells: minority carrier diffusion and recombination [4]. In standard silicon solar cells, Fermi level splitting occurs at forward bias, being E_{Fn} the electron quasi-Fermi level, and E_{F0} as the equilibrium Fermi level. In this situation, we may define $qV_F = E_{Fn} - E_{F0}$ for forward biased p-n junctions where V_F is the potential associated with the splitting of the Fermi levels, related in our case to the accumulation of minority carriers with density n (electrons) [3]. Using Boltzmann statistics for the electron density the capacitance per unit area associated with the homogeneous accumulation in a layer of thickness L is given by

$$C_\mu = \frac{q^2 L n_0}{k_B T} e^{qV_F/\eta k_B T} \quad (1)$$

where n_0 is the minority carrier density in equilibrium, and η is the diode quality factor.

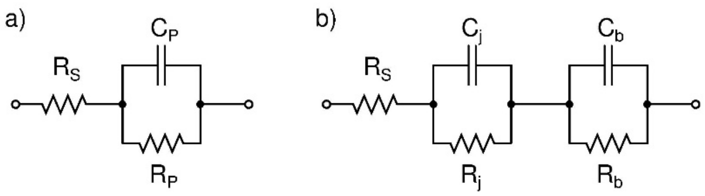

Figure 1. a) Equivalent circuit for IS. b) Equivalent circuit showing junction capacitance C_j as well as pp^+ back contact junction capacitance.

The studied solar cells are fabricated on p-type Si, with a highly P-doped emitter to form the n^+p junction and with a back surface field (BSF) at the back contact forming a pp^+ junction. Impedance spectra will be fitted using the equivalent circuits in figure 1. Part a) shows the simple circuit for a solar cell obtained in the LCR system. Figure 1b shows the equivalent circuit for the AC measurements taking into account both junctions, C_j and R_j for the n^+p junction, and C_b and R_b for the BSF junction. In our model, C_j stands for the chemical capacitance and R_j is the recombination resistance (R_{rec}) given by $R_{rec} = \tau_n / C_\mu$.

For reverse bias, Mott-Schottky behaviour is expected as an excess of majority carriers is present in the n^+p junction. Both the built-in potential V_{bi} and the carrier density N_A may be obtained through the well-known expression

$$C^{-2} = \frac{2(V_{bi} - V)}{A^2 q \varepsilon \varepsilon_0 N_A} \quad (2)$$

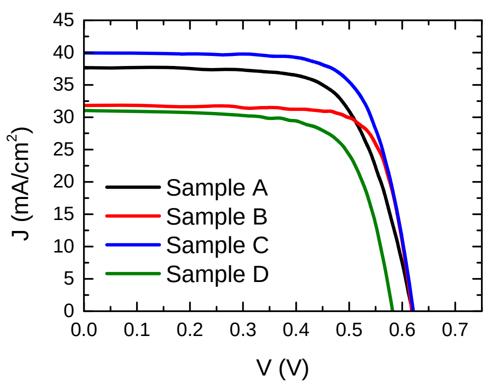

Figure 2. JV characteristics at 1 sun (AM1.5G, 25ºC) of the four solar cells studied in this work.

3. Results and discussion

JV characteristics for the studied samples at 1 sun are shown in figure 1, showing differences mainly in the J_{sc} value, responsible for the differences in power conversion efficiency of the solar cells. Moreover, JV curves do not give enough information to find an explanation to the low V_{oc} value of sample D.

Further characterization of each sample comprises C-V measurements in the dark at different frequencies. 2kHz was chosen for the analysis from the C-f curves for a constant C region, and also far from the cutoff frequency. The experimental results show a linear behaviour of C^{-2} through a wide range of bias voltages, yielding both V_{bi} and N_A after fitting to equation (2). Fitting results are summarized in table 1.

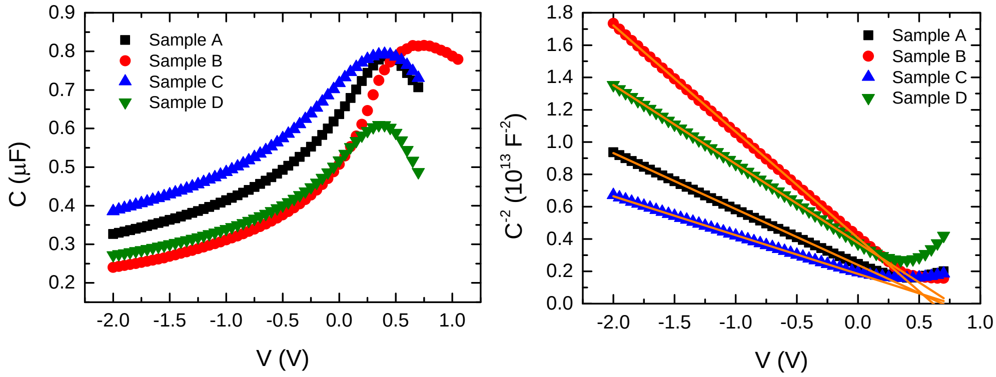

Figure 3. Solar cells dark CV characteristics at a frequency of 2 kHz, and corresponding Mott- Schottky plot with fitting lines to equation (2).

According to equation (1), the junction capacitance should increase as a function of forward bias. However, that is not the case after a given voltage in every analysed sample. It has been shown in classic Schottky diodes [5] that under moderate to large forward bias conditions, minority carrier injection can be limited depending on the barrier heights at the metal–semiconductor junction.

Table 1. CV and DC parameters for the studied cells

Sample	N_A (10^{16} cm^{-3})	V_{bi} (V)	J_{sc} (mA/cm^2)	V_{OC} (mV)
A	1.1	0.69	38.1	617
B	0.9	0.62	33.9	619
C	1.7	0.77	40.0	618
D	0.8	0.77	28.0	516

Next step in solar cell characterization was IS analysis of the samples. Figure 4 summarizes electrical impedance measurements in the complex plane for different voltage bias. After LCR measurements, complex impedance is obtained in the form $Z = Z' + iZ''$. Those values are plotted in a Nyquist plot producing arcs with different amplitudes for each voltage. Those semicircles are easily described by means of the equivalent circuit of figure 1a), and fittings to that model was performed using the *EIS Spectrum Analyser* software [6].

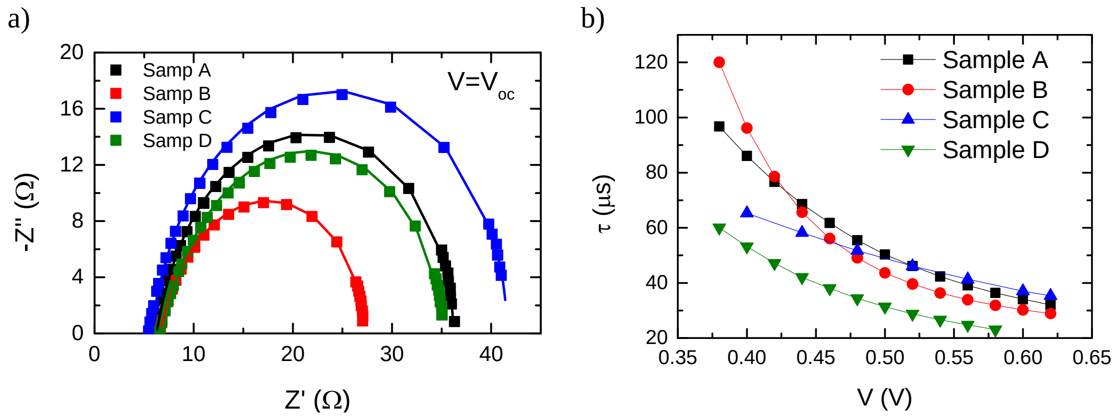

Figure 4. a) Nyquist plot in dark at a voltage equivalent to the V_{oc}. Solid lines are fits to the model of figure 1a) using EIS Spectrum Analyser [6]. b) Electron lifetimes obtained for each sample as a function of cell bias.

Series resistance in the model is the value of the starting point of the imaginary part of the impedance (Z''), which turns out to be very similar in all the cells, in close relation to de DC characterization curves. Moreover, semicircle width is the value of the recombination (junction) resistance and the maximum imaginary impedance corresponds to the product $C_P R_P$ from which the electron lifetime was calculated (figure 4b). The obtained lifetimes at (V_{oc}), are consistent with DC characterization. The contribution of the p–p+ junction is not detected in the impedance spectra for samples A, B and C, until a strong forward bias is applied (not shown here). This is due to the fact that at moderate forward bias, the voltage across the n+–p and p–p+ junctions compresses the space-charge layer, consequently reducing the junction width. However, sample D shows a remarkable asymmetry in the impedance spectrum indicating that BSF capacitance is playing an important role, mainly at high bias voltages.

4. Conclusions

IS analysis has been used as a technique to analyse solar cell behaviour. Different cell parameters, as series and parallel resistances, capacitance, minority carrier lifetime, acceptor impurities density have been obtained as function of applied bias. We showed that electron lifetimes follow DC characteristics in terms of short-circuit current density. It's also been shown that BSF needs to be taken into account to explain the impedance spectrum.

Acknowledgments

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