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Analysis of the aliasing effect caused in hardware-in-the-loop when reading PWM inputs of power converters

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ABSTRACT

Hardware-in-the-loop (HIL) systems are commonly used to debug controllers in closed-loop operation. Therefore, the frequency response of the emulated subsystem is of special relevance. Undesirable oscillations can appear as a consequence of digitally sampling the switch control signals in power converter HIL models. These oscillations at relatively low frequencies, below the switching frequency, may confound the closed-loop operation and, therefore, the appropriate debugging of the controller. This paper shows that the lost information when an HIL model reads a PWM signal may create some output offset error or steady-state fluctuations, especially when the switching period and the sampling step get closer. The aliasing frequencies produced by the input sampling are calculated, and the small-signal analysis explains the relation between the output oscillation and the input PWM sub-harmonics. The output error spectrum proves that the main error sub-harmonics have the same aliasing frequency components. Both captured oscilloscope results obtained by an NI myRIO device and MATLAB simulations verify that significant distortions can be seen in the output inductor current if there is a low aliasing frequency in the digital version of the input PWM signal read by the HIL model.

1. Introduction

Hardware in the loop (HIL) is a prevalent real-time (RT) simulation technique whereby an actual system is interfaced to a virtual part of it implemented into digital hardware (processors, Field Programmable Gate Arrays (FPGAs), etc.) [1–4]. The digital hardware selection depends on both the system complexity and its operating frequency. FPGAs are mainly applied for mid-high switching frequency HIL power electronics applications due to their low input/output latency, fast computing time, and flexibility for designing new circuits [5–7].

HIL designers must take into account several sources of error (inaccurate input reading, inappropriate simulation step, simplification of the model, etc.) that the HIL model can be confronted with since maintaining the accuracy is the primary concern for HIL testing to be reliable [8–10]. The general idea proposed in [11,12] for minimizing the error is achieving the minimum possible time step. Ref. [13] proves that the HIL model accuracy is inversely proportional to the simulation step if the HIL model uses the same mathematical method for solving the equations. Reducing the mathematical complexity can also reduce the time step taking into account that simpler mathematical models may obtain higher errors [14]. Different methods for solving Ordinary Differential Equations (ODE) such as Forward Euler [15], Tustin [16], Adams–Bashforth [17], and Runge–Kutta [18] can be applied to design an HIL model with different precisions [19].

The model designed in hardware proceeds with the rest of the system through input/output analog or digital ports. One kind of inputs in power converter HIL models is the signals sent to the gates of the switches (i.e., PWM inputs), which are digital inputs. These models use a sampling frequency for the digital inputs as high as possible, but cannot detect the exact transition moment. The lost input information can be treated as a sampling error caused by sampling resolution found in HIL models but not real-world systems. It may account for a significant portion of the total error if the input varies with a mid-high frequency [20,21].

In order to avoid the sampling error, both the controller and the HIL model should be implemented in the same device using the same clock signal. However, HIL is intended for debugging any controller in its final implementation. So the HIL model and the controller hardware will be implemented in different hardware devices using different clock signals, and the loss of information will be unavoidable. Several oversampling methods (double-interpolation [22], interpolation extrapolation [23], post-correction [24], and time-averaged method [25]) have been presented for CPU-based HIL applications because of their

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low sampling resolution. The basic concept in these papers is oversampling the input with a frequency higher than the model simulation step to increase the accuracy. They result in a more precise HIL model at the expense of demanding more resources due to their higher level of complexity. The previous studies focus on improving the output precision without a detailed investigation of the sampling error.

Implementing the HIL models in FPGAs allowed designers to discard oversampling methods in many cases since the simulation step of the models designed in FPGAs becomes smaller. FPGA-based HIL model inputs are usually sampled with the same resolutions as their simulation steps, which is recommended to be quite smaller than the switching period for keeping the precision. However, it is still hard to reach that goal in mid-high frequency HIL applications due to the minimum simulation step needed for executing the model equations [26,27].

It is explained in [28] how the spectral differences between the sampled signal and the original one (aliasing distortions) can shift the signal information from one band to other frequency bands. The aliasing problem may arise when the input frequency components are higher than half the sampling frequency, as shown in [29]. As the sampled input in an HIL model may contain some mid-high frequency components higher than the simulation time step, the aliasing phenomenon needs to be studied. This aliasing distortion leads to undesirable steady-state oscillations presented in [30], which is a drawback admitted by HIL manufacturers. For instance, in [31], Typhoon HIL shows steady-state fluctuations for a switching frequency of 20 kHz when the simulation step is 1 μs. Their solution is oversampling the gate drive signals using sampling periods as low as 3.5 ns, much lower than the simulation step (1 μs or 500 ns). In fact, they recommend the oversampling technique for any switched converters working on switching frequencies over 4 kHz [32], although it implies additional computational load and additional latency (an additional time step dedicated for compensation). Furthermore, not all HIL technologies include oversampling.

To the best of the authors' knowledge, a detailed analysis of the error corresponding to transforming the external signal to discrete input in an HIL model has not yet been reported in the literature. However, the aliasing impact is analyzed in other applications [33–35]. Ref. [36] studies the duty cycle perturbation for a PWM Boost converter and its aliased output components. Furthermore, the aliasing effect of a digitally controlled inverter caused by sampling the output current is presented in [37].

As shown in this study, the HIL model accuracy can be degraded through sampling error (aliasing distortion), which may create significant unexpected oscillations in the output, depending on the simulation time step, the input frequency, etc. The small-signal transfer function of the HIL model can be applied to determine the correlation between input aliasing components and the output ripple [38,39].

This paper aims to analyze the input sampling error of the HIL models, including distortion in the frequency domain. The analysis is carried out using a Boost converter as an example application, although the same issue happens in other HIL applications. The input PWM signal sampling error is analyzed since it contains high-frequency harmonics comparing with other inputs in this example, such as the input DC voltage source. It shows that the input PWM sampling aliasing frequencies are the main reason for the Boost converter output steady-state fluctuations. This issue is especially problematic when the switching period and the sampling step become closer, which may even result in instability.

Following this introduction, Section 2 introduces the PWM sampling error for a Boost converter HIL model without electrical losses. The PWM spectrum analysis and its effects on the output state variables such as the inductor current and the capacitor voltage are shown in Section 3. The aliasing oscillation of the output is illustrated by comparing simulations and NI myRIO experimental results with an offline reference model from MATLAB Simulink in Section 4. Finally, conclusions are presented in Section 5 to summarize the idea.

Table 1
Maximum sampling error depending on the PWM switching period and sampling period.

Switching period (ns)	Sampling period (ns)	Maximum sampling error (%)
10000	150	1.5%
10000	500	5.0%
5000	150	3.0%
5000	500	10.0%

2. PWM sampling error

PWM signals are digital, and they are the inputs of HIL models, which are also digital. However, there is a loss of information when an HIL model reads a PWM signal, adversely affecting the HIL model precision. In general, PWM signals have an infinite temporal resolution, e.g., there can be infinite duty cycles (D). However, an HIL model uses a clock to read its inputs, so it obtains information only every clock cycle (dt), as seen in Fig. 1. The sampled PWM read by an HIL model will be named PWMH, the red signals in Fig. 1.

The HIL model can read the correct PWM switching period (T_{sw}) when T_{sw} is a multiple of the dt (synchronous type). In most HIL applications, the control part is separated from the HIL model, and they are not implemented in the same device with the same clock period. A consequence is that the model reads a periodic pattern of the PWMH signal with different frequency components than the original PWM if T_{sw} is not a multiple of the dt (asynchronous type). Even if T_{sw} is a multiple of dt, when DT_{sw} is not a multiple of dt the model may produce an offset sampling error since it cannot read switch on-time precisely (Fig. 1(a)).

The total number of cycles among switching pattern repetitions (N), which is calculated in (1), can be defined as a criterion to distinguish between synchronous and asynchronous categories (LCM stands for Least Common Multiple). In short, N is the number of switching cycles after which the model will reread the same D pattern. In this paper, for the synchronous type, the N value is assumed less than 10 since the HIL model behavior is close to the ideal synchronous case with $N = 1$. If N is greater than 10, the PWMH would belong to the asynchronous type. These two sampling categories are shown in Fig. 1.

$$N = \frac{LCM(T_{sw}, dt)}{T_{sw}} \tag{1}$$

For the ideal synchronous case, the switching period is read correctly, while the switch on-time or off-time can be read with a sampling error up to dt, depending on the exact moment when the PWM changes. However, in the examples with $N > 1$, both on-time and switching period, read by the model, can differ from the original one. The delays between PWM transition and its detection by the HIL model are denoted by E_D (when the PWM signal varies from on to off) and E_T (when the PWM signal varies from off to on) in Fig. 1. Both E_D and E_T shown in this figure have an absolute error range from 0 to dt. They follow a periodic sequence of length N. The maximum possible error in the PWMH signal depends on the switching period and sampling period, as shown in Table 1. It illustrates how different sampling periods affect the precision of PWMH signal. The imprecise D detection can result in some steady-state output fluctuations making the output distorted, as will be discussed in the following.

3. Sub-harmonic oscillations in HIL

This analysis assumes that the original PWM sampling period and the HIL model update period are the same. For instance, if the HIL model simulation step is set to 150 ns (6.67 MHz), the input PWM will be sampled with the same sampling frequency. However, if both periods are not set at the same value, the significant one for this analysis is the PWM sampling period (dt), which would be the smallest of both if they are different.

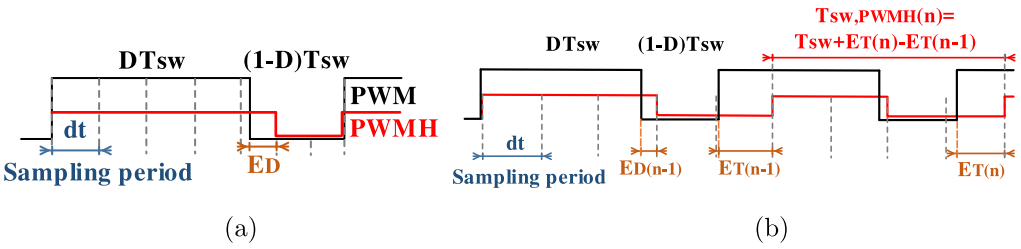

Fig. 1. Input PWM sampling; (a) Synchronous type with $N = 1$, (b) Synchronous or asynchronous type with $N > 1$.

Eq. (2) calculates the sub-harmonic frequencies produced by input PWM sampling with the HIL model simulation step ($f_{aliasing}$). When N value is high and k is small, low-frequency components may arise that may produce critical steady-state oscillations. Since the Boost converter is a low-pass filter, mid-high frequency PWMH sub-harmonics will be naturally filtered in its output, so they do not become a problem. However, the PWMH low-frequency subharmonics may play a significant role in the error. Although the application example in this paper is a Boost converter, this analysis would be exactly the same for other power converters. The implied frequencies, $f_{aliasing}$, do not depend on the specific topology of the converter, but only on the switching period and sampling period relation. Furthermore, all power converters are designed for filtering frequencies over the switching frequency, but oscillations at frequencies under it will be a problem for any topology.

$$f_{aliasing} = \frac{k}{N \cdot T_{sw}}, \qquad for\ k = 1, 2, 3, \ldots \tag{2}$$

Asynchronous PWM sampling may create some sub-harmonics ($f_{aliasing}$), which the HIL system cannot tolerate if they appear. In Table 2, four cases are introduced to clarify the aliasing distortion in HIL systems. The only synchronous example in this paper is case 1, in which the model samples the external 100 kHz PWM signal with a resolution of 150 ns (the minimum achievable time step of the Boost model designed in the NI myRIO device). Case 2 demonstrates how a slight change in the PWM switching period (from 10000 ns to 10001 ns) can convert a synchronous case to an asynchronous one. In case 3, dt is modified to 500 ns, which is a usual time step in recent commercial HIL systems. Case 4 is presented to show that the aliasing phenomenon can be significant in HIL systems even if dt is small. D_1 and D_2 in each case correspond to duty cycles resulting in insignificant and significant PWMH sub-harmonics, respectively.

The harmonic spectrum analysis of the PWMH signal for different case studies is shown in Fig. 2. As can be seen in this figure, changing D does not affect the involved frequencies in the input sub-harmonics when dt and T_{sw} are constant. However, varying the duty cycle does influence the amplitude of the PWMH sub-harmonics. This figure verifies that lower frequency components can be found in the PWMH signal as N increases. Furthermore, when dt increases (case 3), the sub-harmonics amplitudes can also increase.

The Fourier series of the original PWM, which is an even signal, is calculated with the formula given in (3). Despite the fact that the input PWM has only odd harmonics corresponding to T_{sw}, the PWMH signal includes all aliasing frequencies shown in (2). This is due to the PWM signal sampling, which depends on the sampling resolution and the PWM period.

$$PWM(t) = \frac{1}{2} + \sum_{n=1}^{\infty} \frac{1}{n\pi} sin\frac{2n\pi}{T_{sw}}t, \quad for\ n = 1, 3, 5, \ldots \tag{3}$$

The effects of aliasing sub-harmonics can be analyzed by obtaining the small-signal transfer function of the duty ratio to the state variables. The duty cycle to inductor current and capacitor voltage small-signal transfer functions ($\tilde{i}_l(s)/\tilde{d}(s)$ and $\tilde{v}_c(s)/\tilde{d}(s)$) of the Boost converter with a resistive load (R_O) are expressed in Eqs. (4) and (5), respectively:

$$\frac{\tilde{i}_l(s)}{\tilde{d}(s)} = \frac{R_O C V_C\ s + 2V_C}{R_O LC\ s^2 + L\ s + (1-D)^2 R_O} \tag{4}$$

$$\frac{\tilde{v}_c(s)}{\tilde{d}(s)} = \frac{-LV_C\ s + (1-D)^2 R_O V_C}{(1-D)(R_O LC\ s^2 + L\ s + (1-D)^2 R_O)} \tag{5}$$

where the nominal capacitor voltage (V_C) can be calculated by (6). The nominal values of the inductor (L), the capacitor (C), the duty cycle, the input voltage (V_{in}), and R_O used in this paper are considered 800 μH, 80 μF, 0.4, 12 V, and 12 Ω, respectively. In order to predict the frequency response that corresponds to these small-signal transfer functions, the bode plots (the magnitude and phase frequency response) are drawn in Fig. 3. As can be seen, the Boost converter is a low pass filter in which the sub-harmonics up to 1 kHz pass to the output with a higher gain. These sub-harmonics can be the main source of the error, as will be discussed in Section 4.

$$V_C = \frac{V_{in}}{(1-D)} \tag{6}$$

The harmonic spectrum of the inductor current is illustrated in Fig. 4 as an example to demonstrate the effects of the input PWMH sub-harmonics on state variables (the same analysis can be accomplished for the capacitor voltage). As can be seen, the inductor current spectrum has the same frequency components as the PWMH signal. Furthermore, the sub-harmonics amplitudes for asynchronous cases are bigger when the chosen D causes a high-amplitude oscillation. As expected, the amplitude of each sub-harmonic component is the multiplication of the corresponding sub-harmonic in the input (see Fig. 2) multiplied by the gain of the transfer function for that frequency (see Fig. 3). Although the analysis has been carried out using a Boost converter as an application example, the same analysis can be easily adapted to any other power topology. In order to get the final sub-harmonic oscillations in the current or voltage of any converter, the sub-harmonic components in the input (Fig. 2), which do not depend on the topology, would be multiplied by the frequency response of the specific converter (Fig. 3), which is just the Bode plot of the converter. Therefore, the same methodology can be easily applied to any power converter, and similar results would be achieved since all power converters are designed to filter frequencies over the switching one, but not under it. The next section will present the model error spectrum to verify the PWMH sub-harmonics role in total error.

4. Simulation and experimental results

In this section, a set of simulations and experiments has been carried out on a Boost converter HIL model with an external input PWM signal affected by the aliasing distortion to clarify the error caused by the input's inaccurate PWM control signal reading. The nominal values of different parameters used for the simulation and experiments are the same as those selected in the previous section.

Firstly, the Boost converter HIL model was simulated in MATLAB. The simulated model reads the original input PWM signal with a resolution of dt presented in Table 2. The same model with a time step of 1 ns was used to represent the reference model as it is more accurate than the model under test. This time step cannot be used in real-time tests because it is smaller than the HIL model minimum achievable clock period. The reference model avoids the aliasing phenomenon (low-frequency steady-state oscillation in the output, which is not

Table 2
Different case studies and the fundamental aliasing frequency.

Case	T_{sw} (ns)	dt (ns)	D_1	D_2	N	$f_{aliasing}$ (Hz)	Type
1	**10000**	**150**	**0.410**	**0.411**	3	33333	Syn
2	**10001**	**150**	**0.400**	**0.403**	150	666.6	Asyn
3	**10001**	**500**	**0.400**	**0.416**	500	199.98	Asyn
4	**9901**	**150**	**0.409**	**0.400**	150	673.3	Asyn

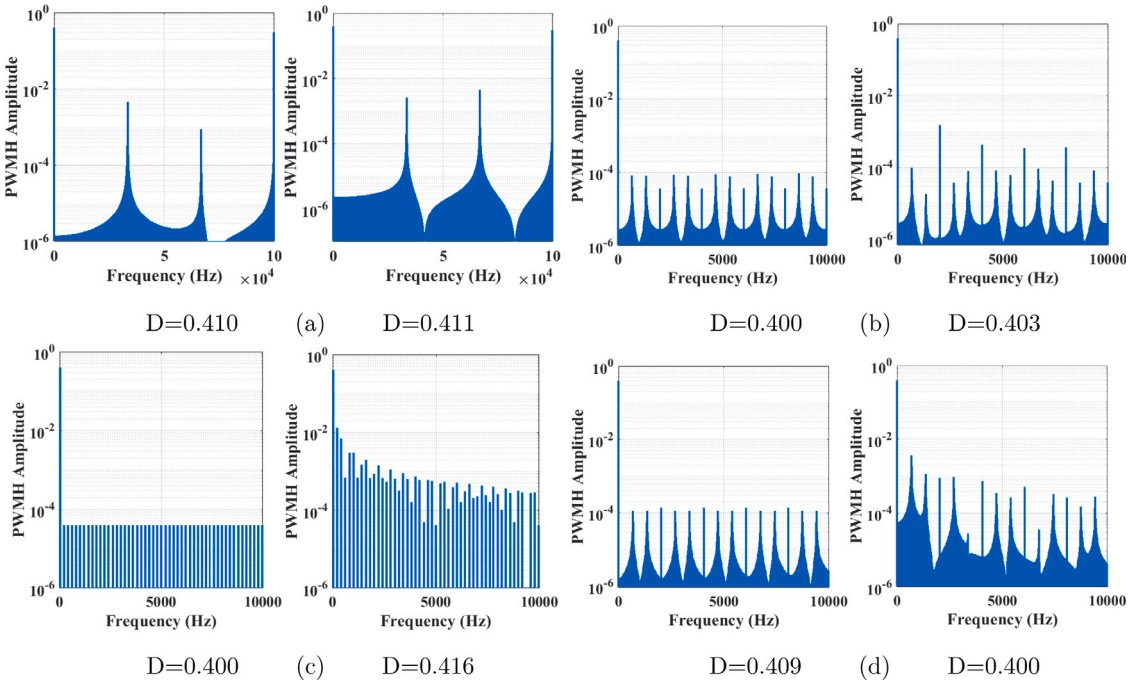

Fig. 2. The harmonic spectrum of the PWMH signal for two different D obtained by MATLAB simulation; (a) Case 1: T_{sw} = 10000 ns & dt = 150 ns, (b) Case 2: T_{sw} = 10001 ns & dt = 150 ns, (c) Case 3: T_{sw} = 10001 ns & dt = 500 ns, (d) Case 4: T_{sw} = 9901 ns & dt = 150 ns.

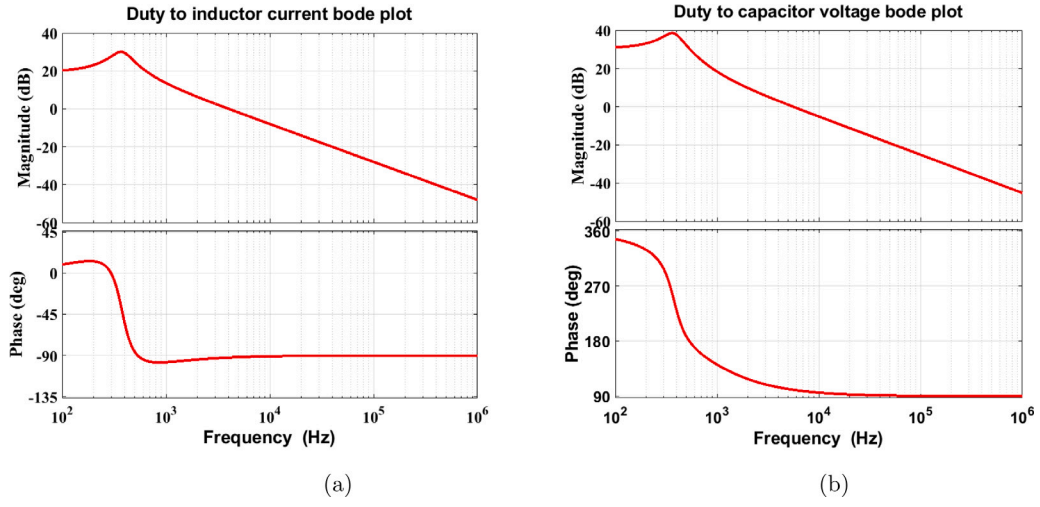

Fig. 3. The state variables bode plots; (a) control to inductor current, (b) control to capacitor voltage.

supposed to be seen in real systems) since all tested switching periods are multiples of its time step with $N = 1$.

As shown in Fig. 5, state variables errors can be totally different when D sweeps from 0.4 to 0.5 even if the switching period is constant. Thus, it is necessary to analyze the state variables waveforms when the D error is large on the one hand or negligible on the other hand for each case study to demonstrate the behavior of the model in different conditions. The following simulations and experimental tests focus on the steady-state inductor current to clarify the error caused by the aliasing distortion, but a similar analysis can be accomplished for all state variables.

In case 1, N equals three, which means that the time interval of three switching cycles (30000 ns) is a multiple of the time step (150 ns). So, the PWM signal pattern read by the model repeats every 30000 ns. For synchronous cases, N's value is less than 10, resulting in an offset error depending on the D value. For instance, for D = 0.411 and T_{sw} = 10000 ns, the on-time is 4110 ns. Reading it with dt = 150 ns, it can be read as 4050 or 4200 ns. There are two possible patterns for

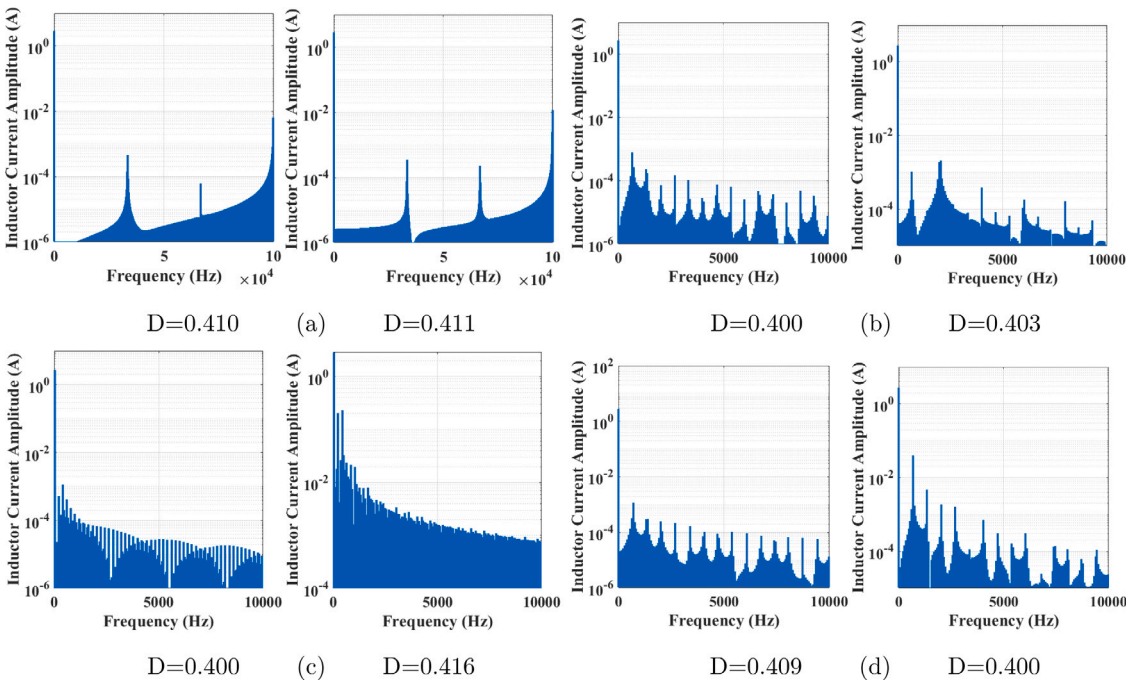

Fig. 4. The steady-state inductor current harmonic spectrum obtained by MATLAB simulation; (a) Case 1: T_{sw} = 10000 ns & dt = 150 ns, (b) Case 2: T_{sw} = 10001 ns & dt = 150 ns, (c) Case 3: T_{sw} = 10001 ns & dt = 500 ns, (d) Case 4: T_{sw} = 9901 ns & dt = 150 ns.

this specific case depending on the PWM initial phase. Every $N = 3$ cycles, the pattern will repeat: 4200, 4200, 4050 or 4050, 4050, 4200 with the average on-time of 4150 or 4100 ns instead of 4110 ns. Thus, an offset (+40 or −10, respectively) is generated, taking into account that it cannot exceed dt/N (50 ns in this example). When N is large enough, the average of N on times can accurately represent any average value. However, the pattern to get that value can be very long, taking up to $N \cdot T_{sw}$. That is why sub-harmonic oscillations appear for asynchronous cases but almost no offset.

A comparison between case 2 and case 3 in Fig. 5 proves that decreasing the sampling resolution will increase the mean absolute error (MAE) of the model. However, big sub-harmonic oscillations are not exclusive of longer dt. As shown in case 4, a higher MAE error can be obtained even if the input is sampled with the same sampling period (dt = 150 ns) of cases 1 and 2.

Fig. 6 shows the MATLAB simulation results of the inductor current in steady-state for different case studies discussed in this paper. As can be seen, synchronous cases (case 1) may result in a more significant error than asynchronous ones (case 2). However, the offset error can be compensated by the regulator. The offset error is inversely proportional to the N value, which means the bigger N is, the smaller the achieved offset error is. If N is greater than 10, the model will face an asynchronous scenario in which a permanent oscillation can be detected, as shown in cases 2, 3, and 4. The oscillation amplitude, which is the primary source of the error in asynchronous cases, depends highly on the sampling period and the switching period. When they are relatively closer, the model will face visible oscillations, as depicted in case 3. Notably, high-amplitude fluctuations can be seen in case 4, although its peak-to-peak oscillation is not as huge as in case 3. These unintended distortions can confuse the controller and prevent its proper operation.

The MAE of the inductor current, the capacitor voltage, and the duty cycle for tested case studies are calculated in Table 3, where the capacitor voltage, the inductor current, and the duty cycle errors are denoted by e_v, e_i, and e_D, respectively. As shown in this table, the MAE value for synchronous cases is not always bigger than asynchronous cases. For instance, a higher percentage of inductor current error is observed in case 4, although case 2 has less error than the synchronous case study (case 1). The highest value of e_D is obtained for case 3 when $D = 0.416$ since its sampling resolution is 3.3 times less than in the other cases. Nevertheless, as can be seen, even its bigger dt will not result in a significant error for all Ds.

Table 3
The percentage steady-state error of the model.

Case	T_{sw} (ns)	D	e_i	e_v	e_D
1	**10000**	**0.410**	0.0375	0.0082	0.5278
		0.411	1.3503	0.6893	0.5244
2	**10001**	**0.400**	0.0588	0.0133	0.4049
		0.403	0.1511	0.0329	0.2395
3	**10001**	**0.400**	0.1151	0.0324	0.0034
		0.416	12.5076	4.6137	2.1717
4	**9901**	**0.409**	0.7000	0.0161	0.0229
		0.400	1.8610	0.5428	0.7221

In Fig. 7, the inductor current error harmonic spectrum for different case studies is shown to find the main error frequency components. For the synchronous case, the primary error component is in 0 Hz (the offset error) for both D, although it is more evident in the case with $D = 0.411$. In case 2, there is no clear dominant frequency component (a component whose amplitude is ten times greater than the rest) involved in the inductor current error. The same scenario happens for cases 3 and 4 when D is 0.4 and 0.409, respectively. However, in case 3 with $D = 0.416$ or in case 4 with $D = 0.4$, there is at least one obvious dominant frequency in the error, which can be seen as a sub-harmonic oscillation in the inductor current (see Fig. 6). This undesirable effect may cause considerable distortions in HIL models (cases 3 and 4).

Notably, the synchronous cases with only offset error can just be seen in the simulation, not the experiments. The reason is the unideal input PWM signal, whose switching period cannot be precisely a multiple of the time step with little N values. A slight modification of the switching period can generate a low-frequency high-amplitude oscillation in the output. For instance, the difference between cases 1 and 2 is just one nanosecond in their switching periods. However, this small change (0.01%) of the switching period results in a permanent fluctuation caused by the aliasing frequencies.

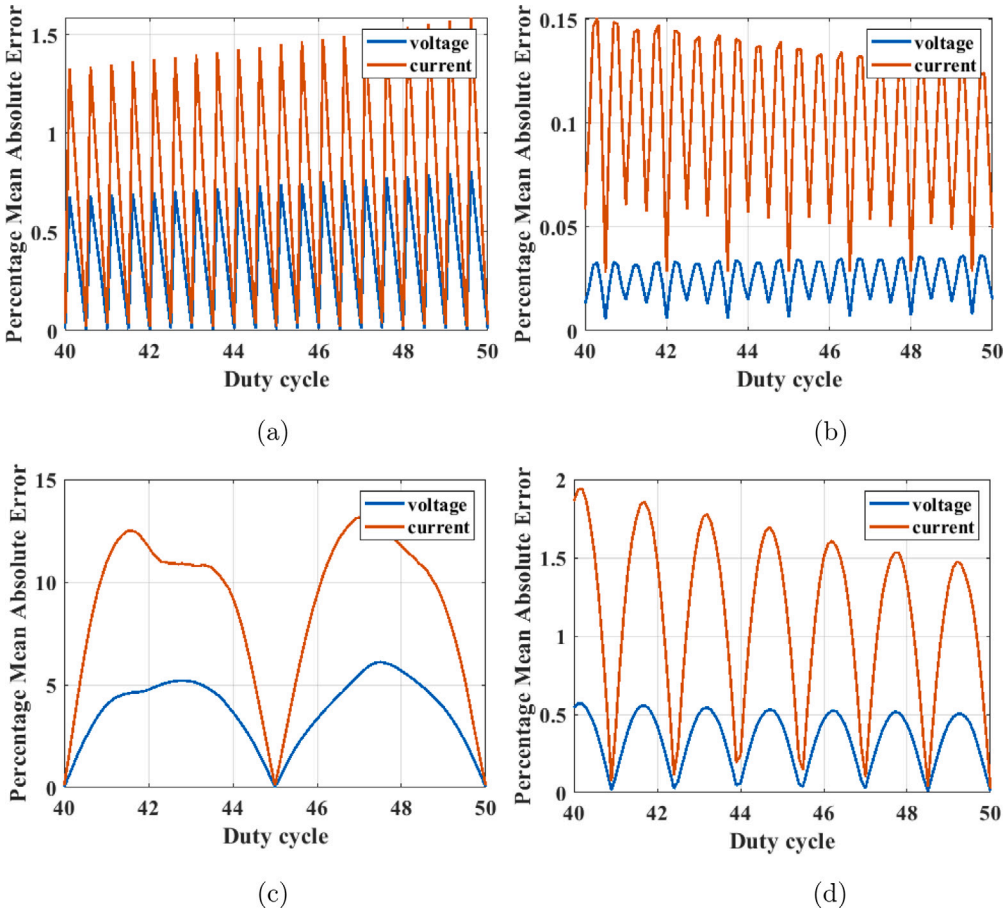

Fig. 5. The inductor current and capacitor voltage percentage mean absolute error versus duty cycle; (a) Case 1: T_{sw} = 10000 ns & dt = 150 ns, (b) Case 2: T_{sw} = 10001 ns & dt = 150 ns, (c) Case 3: T_{sw} = 10001 ns & dt = 500 ns, (d) Case 4: T_{sw} = 9901 ns & dt = 150 ns.

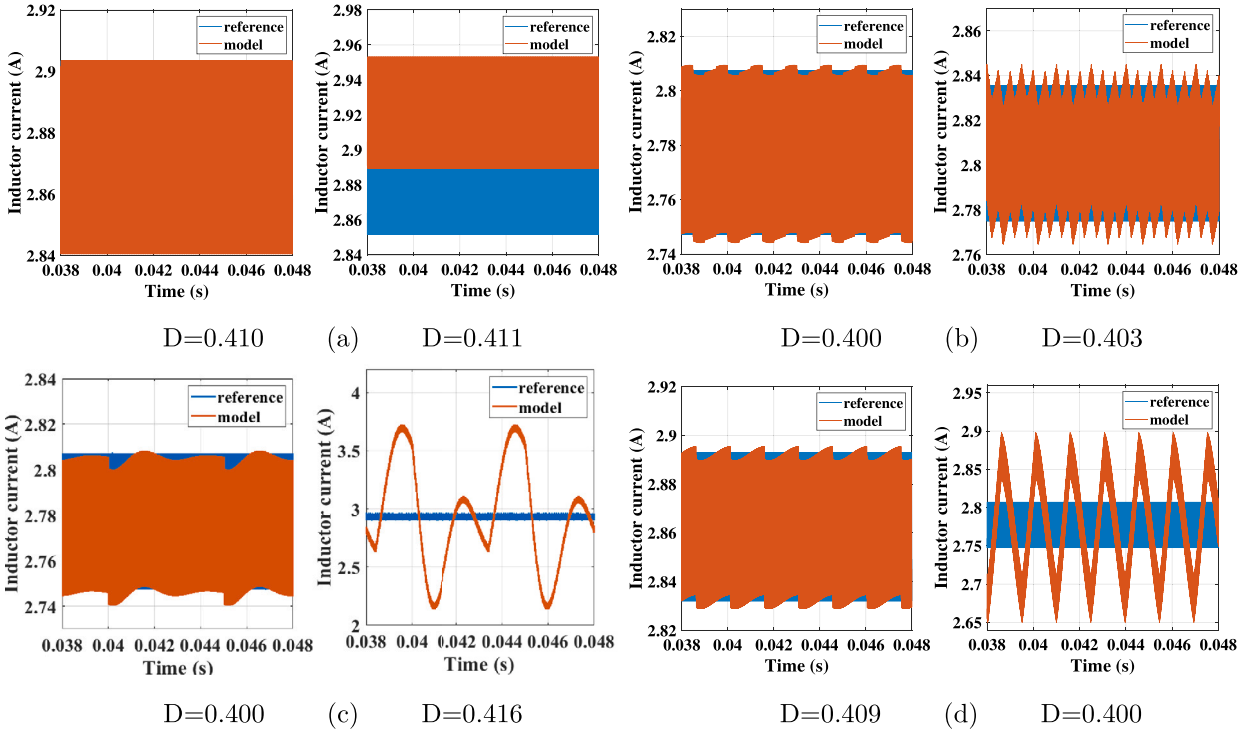

Fig. 6. The steady-state inductor current obtained by the MATLAB simulation; (a) Case 1: T_{sw} = 10000 ns & dt = 150 ns, (b) Case 2: T_{sw} = 10001 ns & dt = 150 ns, (c) Case 3: T_{sw} = 10001 ns & dt = 500 ns, (d) Case 4: T_{sw} = 9901 ns & dt = 150 ns.

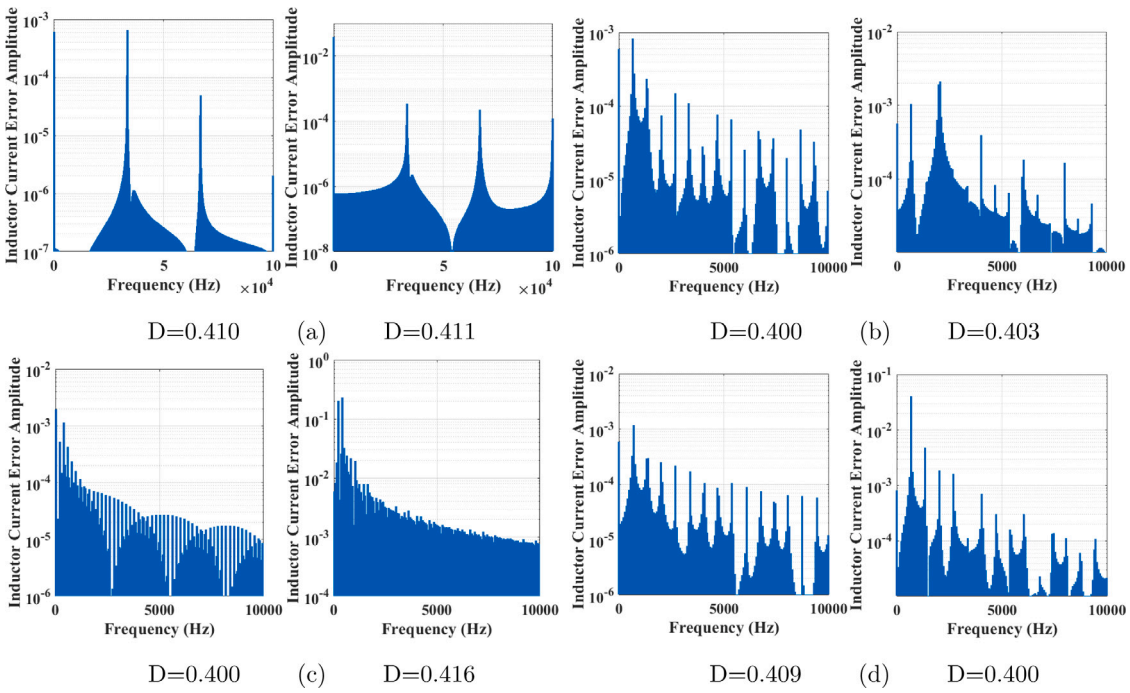

Fig. 7. The inductor current error harmonic spectrum; (a) Case 1: T_{sw} = 10000 ns & dt = 150 ns, (b) Case 2: T_{sw} = 10001 ns & dt = 150 ns, (c) Case 3: T_{sw} = 10001 ns & dt = 500 ns, (d) Case 4: T_{sw} = 9901 ns & dt = 150 ns.

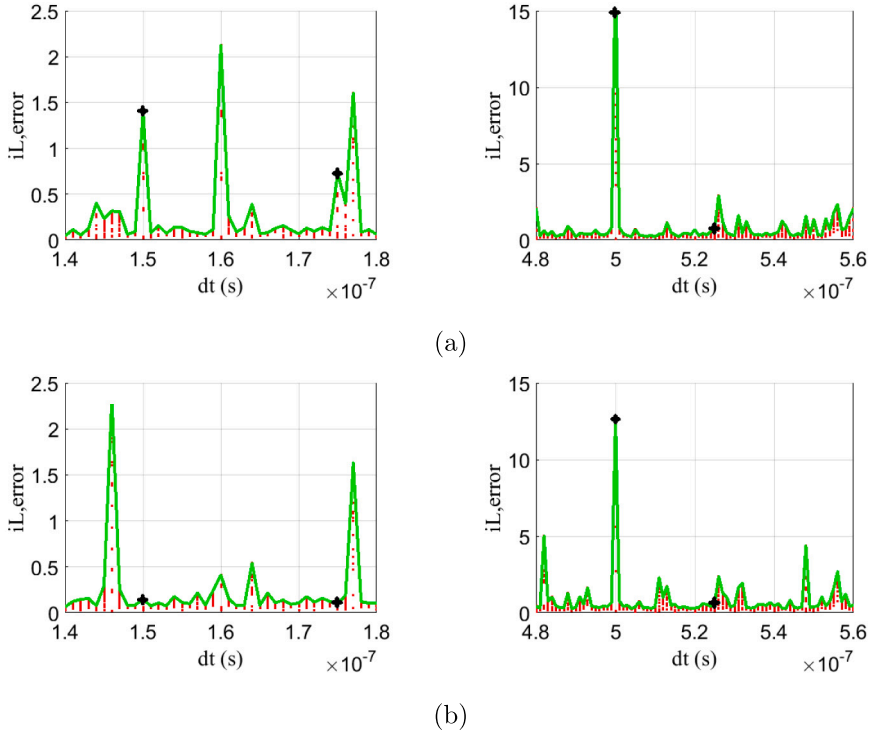

Fig. 8. The inductor current MAE sweeping duty cycle versus dt; (a) T_{sw} = 10000 ns, (b) T_{sw} = 10001 ns.

When there is a high-amplitude PWMH sub-harmonic in the frequency range where the model gain is high, a high-amplitude oscillation can be observed, such as cases 3 and 4. An obvious solution would be to drastically decrease dt (at least an order of magnitude), so N also decreases and the PWMH sub-harmonics move out of the high gain zone in the model. However, the simulation step is usually near the technology limit, so it cannot be drastically reduced. A solution is only to decrease the sampling period of the PWM inputs, using oversampling as proposed in [31]. Since the model reads the PWM inputs more accurately, the PWMH sub-harmonics amplitudes will decrease, which results in fewer output oscillations. However, the additional computation load due to the oversampling algorithm complexity and the additional latency in the form of an additional time step dedicated for compensation of each variable are two main drawbacks of the oversampling method. A similar idea is presented by [25,40–42] using

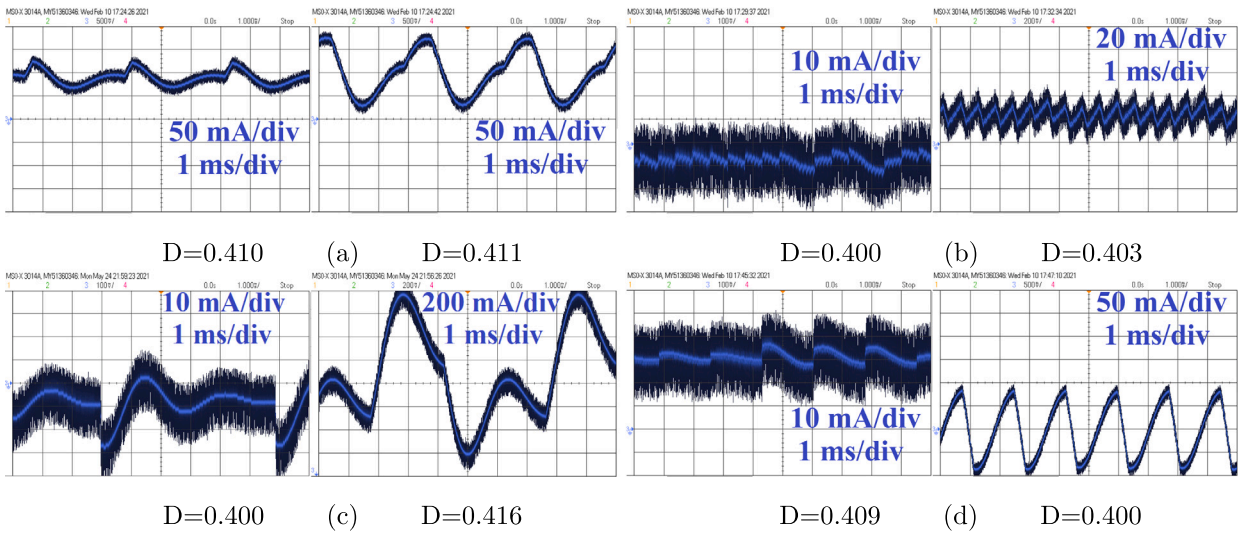

Fig. 9. The steady-state inductor current obtained by NI myRIO device; (a) Case 1: T_{sw} = 10000 ns & dt = 150 ns, (b) Case 2: T_{sw} = 10001 ns & dt = 150 ns, (c) Case 3: T_{sw} = 10001 ns & dt = 500 ns, (d) Case 4: T_{sw} = 9901 ns & dt = 150 ns.

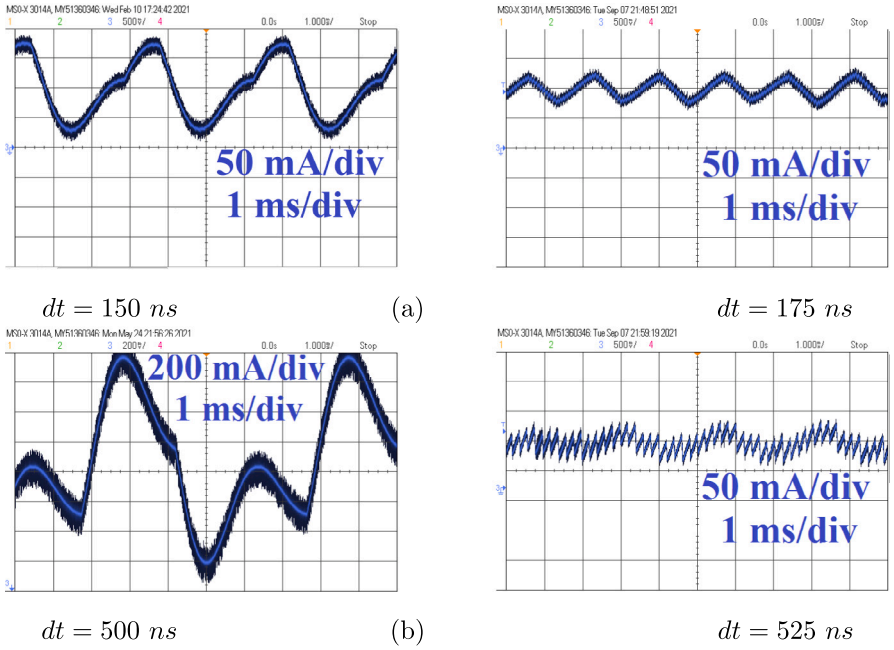

Fig. 10. The steady-state inductor current obtained by NI myRIO device changing dt slightly; (a) T_{sw} = 10000 ns & D = 0.411, (b) T_{sw} = 10001 ns & D = 0.416.

the sub-cycle averaging method to get the maximum resolution of the PWM signal inside the HIL model. Another possible solution would be to make slight variations in dt as needed. In some cases, a small increase in dt may improve the accuracy, as it can shift the high-amplitude PWMH sub-harmonics to the frequency range with higher attenuation, diminishing the total error.

Fig. 8 plots the inductor current error versus dt. The error corresponds to each dt is calculated for duty cycles between 0.4 and 0.46 with the step of 0.02 (cloud points in red color). The green envelope curve represents the maximum error obtained for each dt. According to this envelope curve, there are some dt values that lead to large errors (large sub-harmonic oscillations), but many other dt values obtain much lower errors. It can be seen that slightly modifying dt can drastically decrease the error. For example, changing dt from 500 ns to 525 ns reduces the error by about 20 times. Values 500 and 525 ns are chosen as examples because the experimental results, shown later, are implemented in a hardware device that only admits multiples of 25 ns. As a conclusion of Fig. 8 analysis, all error peaks for dt values around 500 ns (right graphs) are considerably bigger than those for values around 150 ns (left graphs). Furthermore, big error peaks appear only for very specific dt values. Small changes in dt can drastically reduce the problem.

The Boost HIL model has been coded in LabVIEW using a graphical programming language in order to get a hardware implementation in an NI myRIO-1900 device to verify the effects of the aliasing issue observed in the simulation. The experimental validation was performed by connecting an external PWM signal generator to the HIL model of the Boost converter implemented in the NI myRIO device. In this case, the latency of the model designed in LabVIEW to be implemented into the NI myRIO's on-board FPGA (Xilinx Zynq-7010) is six clocks that must be equal to the PWM sampling period. As the on-board FPGA clock period is 25 ns, the PWM sampling period equals 150 ns. Thus, all simulation results have been obtained using time steps equal to or

Table 4
The steady-state inductor current peak-to-peak oscillation for the simulation and the experimental results.

Case	T_{sw} (ns)	D	$i_{L,P-P}$	
			Simulation	Experimental
1	**10000**	**0.410**	≃ 0 mA	85 mA
		0.411	≃ 0 mA	160 mA
2	**10001**	**0.400**	4 mA	10 mA
		0.403	12 mA	20 mA
3	**10001**	**0.400**	10 mA	30 mA
		0.416	1.5 A	1.4 A
4	**9901**	**0.409**	6 mA	10 mA
		0.400	175 mA	190 mA

greater than 150 ns, which are multiples of 25 ns to be equivalent to the experimental results.

As shown in Fig. 9, high-amplitude steady-state oscillations can be observed in the experimental setup. The peak-to-peak inductor current oscillation ($i_{L,P-P}$) discarding the switching ripple oscillation, which is unavoidable, is calculated in Table 4 to compare the simulation and experimental results. For the sake of clarity, Fig. 9 represents only the minimum current value for every switching period since the current ripple is in some cases bigger than the sub-harmonic oscillation. An incompatible result can be seen in case 1, in which the experimental waveform shows a high-amplitude fluctuation, while the simulation does not verify it. As expected, not only the permanent oscillation is observed in the asynchronous cases but also in the experimental synchronous case. The reason is that a perfect synchronous case cannot be found in a real setup, as any tiny difference in the frequencies makes the case asynchronous likely with a big N value. However, in the asynchronous cases, the experimental waveforms support the simulation results.

To confirm the results of Fig. 8, where the relation between dt and sub-harmonic oscillations was theoretically analyzed, the following experimental results are added in Fig. 10. Using the same switching period (10000 or 10001 ns), dt is slightly changed: from 150 to 175 ns, and from 500 to 525 ns. The maximum found oscillations for each combination are shown in Fig. 10. As can be seen, the oscillations are reduced using $dt = 175$ ns instead of 150 ns, and the same for 525 ns instead of 500 ns. These results confirm the results of Fig. 8, showing that big sub-harmonic oscillations appear at very specific dt values, while other similar dt values get much smaller oscillations. Furthermore, the values of the peak oscillations are bigger for bigger dt values (bigger peak oscillations for dt values around 500 ns than for values around 150 ns).

In conclusion, big sub-harmonic oscillations may appear at specific values of dt and D. They always appear for synchronous cases (N values under 10), but appear in only some asynchronous cases. So the first recommendation is to avoid synchronous cases. Regarding asynchronous cases, as big sub-harmonic oscillations appear at only some dt values, a possible solution would be to slightly change dt when big sub-harmonic oscillations are detected. Another conclusion is that the peak values of sub-harmonic oscillations are smaller for smaller dt ranges. So another possible solution would be to use very small dt values. Since drastically decreasing a HIL model time step is not possible, the solution would be to decrease the sampling period without decreasing the model time step, i.e., using oversampling. However, the model must handle the extra information obtained through oversampling, increasing the model complexity.

5. Conclusion

This paper has investigated the aliasing phenomenon caused by the sampling of the input PWM in HIL systems. Four different cases have been introduced, including several switching periods, sampling resolutions, and duty cycles. Some steady-state output oscillations with frequency components similar to the calculated aliasing frequencies produced by the input PWM signal sampling have been observed. When the oscillations become large enough, the validity of the HIL model is jeopardized, making the results less meaningful or even confusing. It has been demonstrated that the inductor current can present sub-harmonic oscillations up to 190 mA and 1.4 A (nominal current 2.8 A) when dt is 150 and 500 ns, respectively. The inductor current error spectrum verified that the main error component corresponds to the calculated fundamental aliasing frequency. The results have been verified by a close match between the simulation and the experiment for all asynchronous cases.

The simulation results show that synchronous cases should only suffer from an offset in the model outputs. However, there are still unavoidable steady-state fluctuations in the experimental results of supposedly synchronous cases, as no perfect synchronous cases can be achieved in a real setup. Therefore, all synchronous cases lead to big sub-harmonic oscillations in real experiments and should be avoided.

If high amplitude steady-state oscillations are found in the output, a first solution would be decreasing dt. However, real-time constraints usually cause that dt cannot be further decreased, unless oversampling techniques are used, increasing the complexity of the model. However, a small increase in dt may be an option since it may locally degrade the error by alleviating the aliasing oscillations. Any change in dt may lead to a decrease in N, increasing the frequencies of sub-harmonic oscillations. Higher frequencies will be naturally filtered by the power converter, decreasing the problem.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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